DESIGN GUIDE

Carrier Board

for VIA QSM-8Q60 Qseven™ ARM module

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Tested To Comply
With FCC Standards
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Revision History

Revision	Date	Description
1.00	03/07/2017	Initial release
1.01	09/02/2020	Updated VIA logo and copyright year

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1. Introduction

This document provides design guidelines to the developers of a custom Qseven compliant carrier board that supports the features of VIA QSM-8Q60™ module. This document includes the layout and routing guidelines for general board designs and major underlying interfaces such as PCI Express, Gigabit Ethernet, USB, LVDS, HDMI and Audio. In addition, the document includes the mechanical information of the ruggedized MXM connector that provides high speed interfaces between the carrier board and the module.

Please note that this document is considered to be a reference guide only. This document is not intended to be a specification. All information and examples listed below are considered to accurate as of the publication date; however developers must be aware that this document is only a referencing guide.

1.1. Document Overview

A brief description of each chapter is given below.

Chapter 1: Introduction

Briefly introduces the structure of the design guide document.

Chapter 2: General Carrier Board Recommendations

General design schemes and recommended layout rules are shown in this chapter.

Chapter 3: Qseven Specification Overview

Detailed information about the MXM connector placement and dimensions are described.

Chapter 4: Layout and Routing Recommendations

Detailed layout and routing guidelines for each major interface are described.

Appendix A: Carrier Board Reference Schematics

Reference schematics of COMEDB2 evaluation carrier board.

1.2. Acronyms and Definitions

Term	Description
ASIC	Application-Specific Integrated Circuit
EMI	Electromagnetic Interference
GBE	Gigabit Ethernet
HDMI	High-Definition Multimedia Interface
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IO	Input/Output
I^2S	Integrated Interchip Sound / Inter-IC Sound
LAN	Local Area Network
LCD	Liquid Crystal Display
LVDS	Low-Voltage Differential Signaling
MiniPCIe	Mini PCI Express
MXM	Mobile PCI Express Module
NC	Not Connected / No Connection
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCIe x1	PCI Express one lane
RJ-45	Registered Jack-45
USB	Universal Serial Bus

Table 1: Acronyms and definitions

1.3. Illustrations and Schematics

Illustrations and schematics depicted in this document may show the directional flow of signals. Directional flow is indicated by the pointed ends of the arrow shapes. See Figure 1.

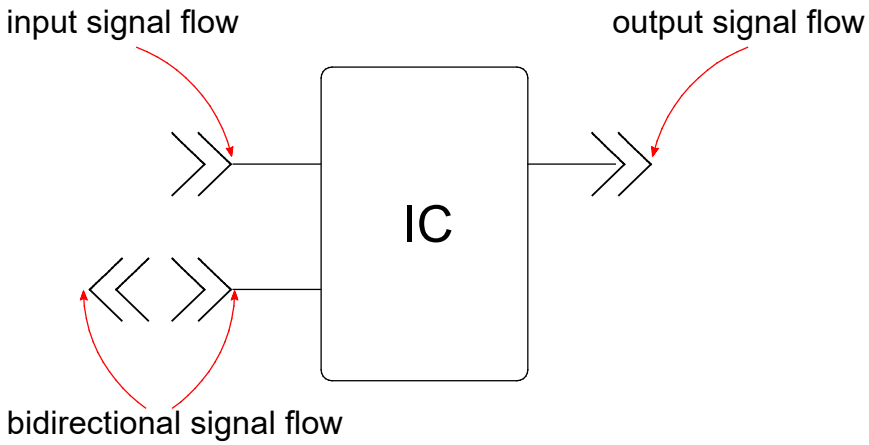

Figure 1: Conventions pertaining to schematics

2. General Carrier Board Recommendations

This section contains general guidelines for the PCB stackup and the layout of traces. General guidelines for routing style, topology, and trace attribute recommendations are also discussed.

2.1. PCB Stackup Example

Figure 2 illustrates an example of a PCB with a six-layer stackup. The stackup consists of three signal layers and three reference (power and ground) layers. The three signal layers are referred to as the component layer, inner layer and solder layer. The example below also shows the PCB stackup in a microstrip design.

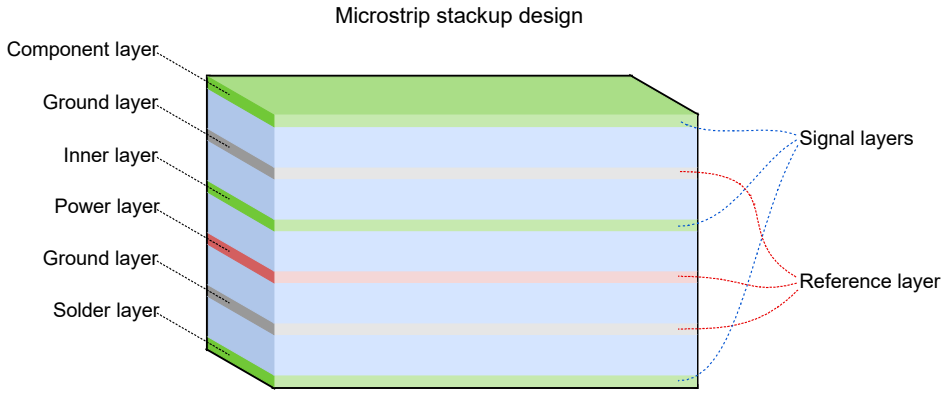

Figure 2: Six-layer microstrip PCB stackup example

2.1.1. Microstrip Versus Stripline Designs

Carrier board designers can choose between two basic categories of PCB design: microstrip and stripline. Microstrip designs have the outer signal layers exposed. Stripline designs have the outermost signal layers shielded by reference layers.

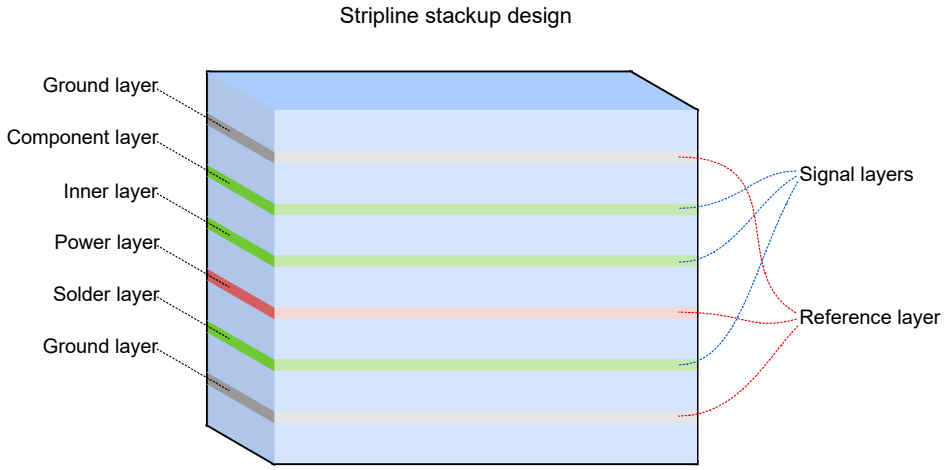

Figure 3: Six-layer stripline PCB stackup example

The choice of microstrip or stripline design depends on the application for which the carrier board is being designed. If the carrier board is being designed for locations where sensitivity to EMI is an issue, a stripline design is recommended for reducing EMI and noise coupling. For applications where the tolerance for EMI levels is greater, a microstrip design is recommended to reduce costs. Due to the inherent nature of stripline PCB stacks, broad-side coupling is possible.

Layer Description	Thickness Value	Spacing (mil)
Component Layer	0.5 oz. Copper + Planting	~62 mils
Prepeg	2.4 ~3.5 mils thickness	
Ground Layer	1.0 oz. Copper	
Prepeg	2.4 ~3.5 mils thickness	
Inner Layer	~52.3 mils thickness	
Prepeg	2.4 ~3.5 mils thickness	
Power Layer	1.0 oz. Copper	
Prepeg	2.4 ~3.5 mils thickness	
Ground Layer	1.0 oz. Copper	
Prepeg	2.4 ~ 3.5 mils thickness	
Solder Layer	0.5 oz. Copper + Planting	

Table 2: General six-layer microstrip PCB stackup

Description	Value	Notes
Dielectric constant (Ɛr) of Prepeg	3.6 ~ 4.2	@ 1GHz
Board Impedance	55Ω ± 10%	For all signal layers

Table 3: PCB stack-up detail

Notes:

1. It is not recommended to have any signal routings on either power layer or the ground layer. If a signal must be routed on the power layer, then it should be routed as short as possible.
2. Signal routing on the ground layer is not allowed.
3. Lower trace impedance providing better signal quality is preferred over higher trace impedance for clock signals.

2.2. General Layout and Routing Guidelines

This section provides general layout rules and routing guidelines for designing carrier boards for VIA QSM-8Q60 module.

2.2.1. Routing Styles and Topology

Topology is the physical connectivity of a net or a group of nets. There are two types of topologies for a motherboard layout: point-to-point and multi-drop. An example of these topologies is shown in Figure 4.

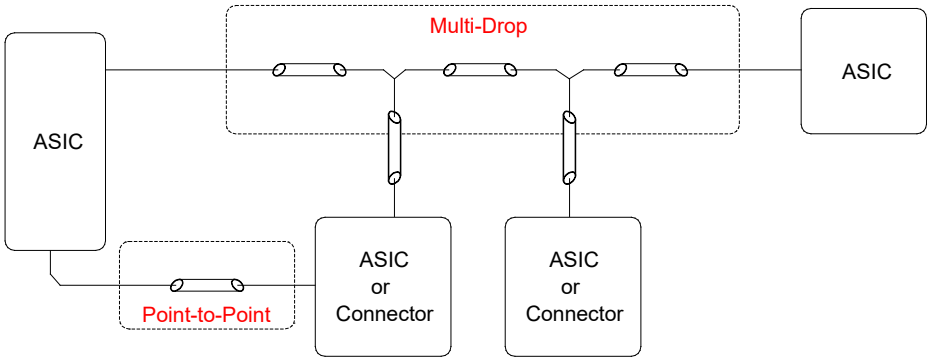

Figure 4: Point-to-point and multi-drop examples

High-speed bus signals are sensitive to transmission line stubs, which can result in ringing on the rising edge caused by the high impedance of the output buffer in the high state. In order to maintain better signal quality, transmission stubs should be kept as short as possible (less than 1.5"). Therefore, daisy chain style routing is strongly recommended for these signals. Figure 5 below shows an example of daisy chain routing.

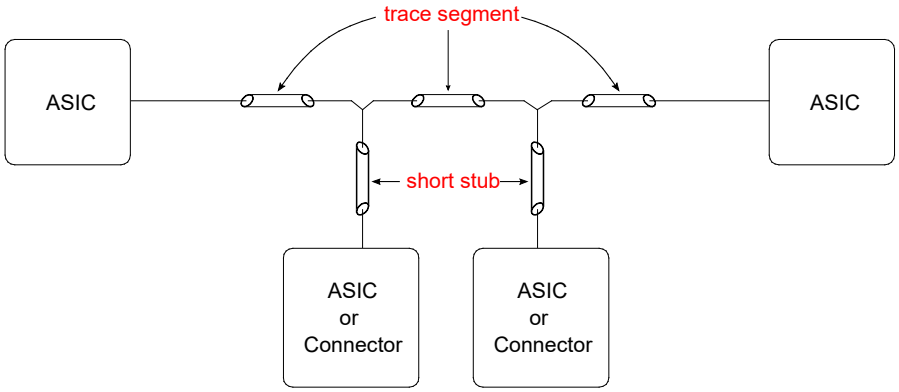

Figure 5: Daisy-chain example

If daisy chain routing is not allowed in some circumstances, different routings may be considered. An alternative topology is shown in Figure 6. In this case, the branch point is somewhere between both ends. It may be near the source or near the loads. Being close to the load side is best. The separated traces should be equal in length.

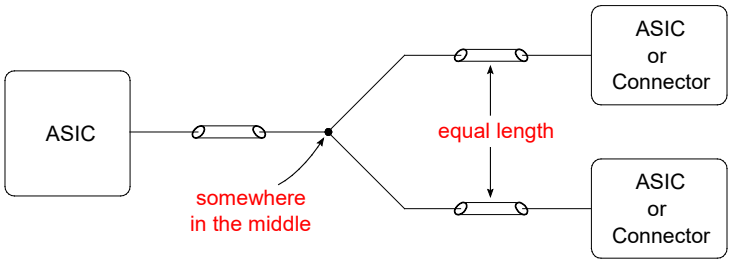

Figure 6: Alternate multi-drop example

2.2.2. General Trace Attribute Recommendations

A 5 mils trace width and 10 mils spacing are generally advised for most signal traces on a carrier board layout. To reduce trace inductance the minimum power trace width is recommended to be 30 mils.

As a quick reference, the overall recommended trace width and spacing for different trace types are listed in Table 4, and the recommended trace width and spacing for each signal group is shown in Chapter 4.

Trace Type	Trace Width (mil)	Spacing (mil)
Regular Signal	5 or wider	10 or wider
Interface or Bus Reference Voltage Signal	20 or wider	20 or wider
Power	30 or wider	20 or wider

Table 4: Recommended trace width and spacing

General rules for minimizing crosstalk in high-speed bus designs are listed below:

- Maximize the distance between traces. Maintain 10 mils minimum spaces between traces wherever possible.
- Maximize the distance (30 mils minimum) between two adjacent routing areas of different signal groups wherever possible.
- Avoid parallelism between traces on adjacent layers.
- Select a board stack-up that minimizes coupling between adjacent traces.

2.2.3. General Clock Routing Considerations

Clock routing guidelines are listed below:

- The recommended clock trace width is 5 mils.
- The minimum space between one clock trace and adjacent clock traces is 20 mils. The minimum space from one segment of a clock trace to other segments of the same clock trace is at least two times of the clock width. That is, more space is needed from one clock trace to others or its own trace to avoid signal coupling (see Figure 7).
- Clock traces should be parallel to their reference ground planes. That is, a clock trace should be right beneath or on top of its reference ground plane (see Figure 8).
- Series terminations (damping resistors) are needed for all clock signals (typically 0 to 47 ohm Ω). When two loads are driven by one clock signal, the series termination layout is shown in Figure 9. When multiple loads (more than two) are applied, a clock buffer solution is preferred.
- Isolating clock synthesizer power and ground planes through ferrite beads or narrow channels (typically 20 mils to 50 mils wide) is preferred.
- No clock traces on the internal layer if a six-layer board is used.

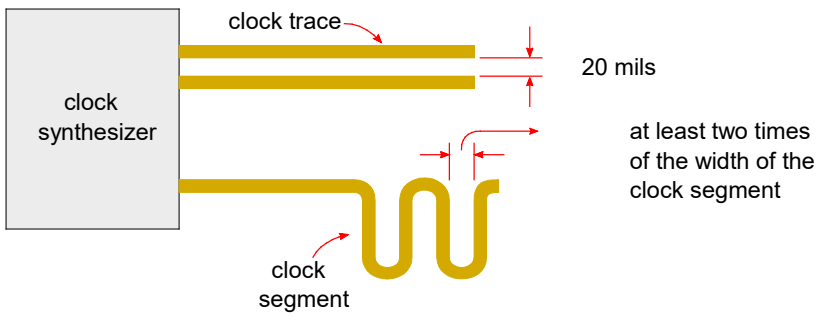

Figure 7: Suggested clock trace spacing

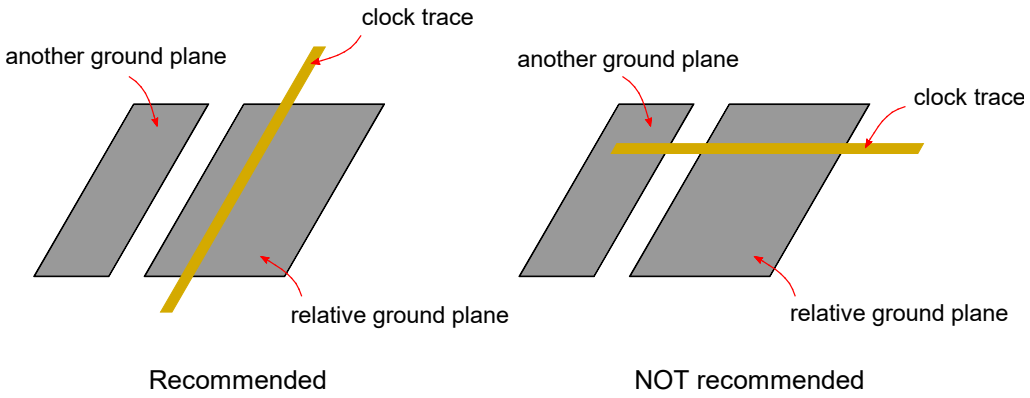

Figure 8: Clock trace layout in relation to the ground plane

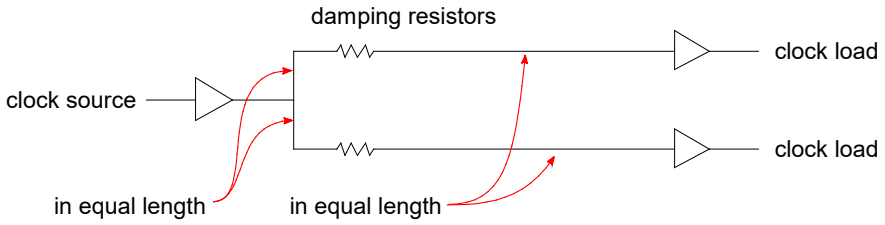

Figure 9: Series termination for multiple clock loads

3. Qseven Specification Overview

The carrier board for VIA QSM-8Q60 module must follow the placement defined in the Qseven specification.

3.1. Qseven Module Placement

Figure 10 shows a depiction of the top view of 3.5" SBC form factor carrier board PCB with appropriate amount of space reserved for the Qseven module (VIA QSM-8Q60).

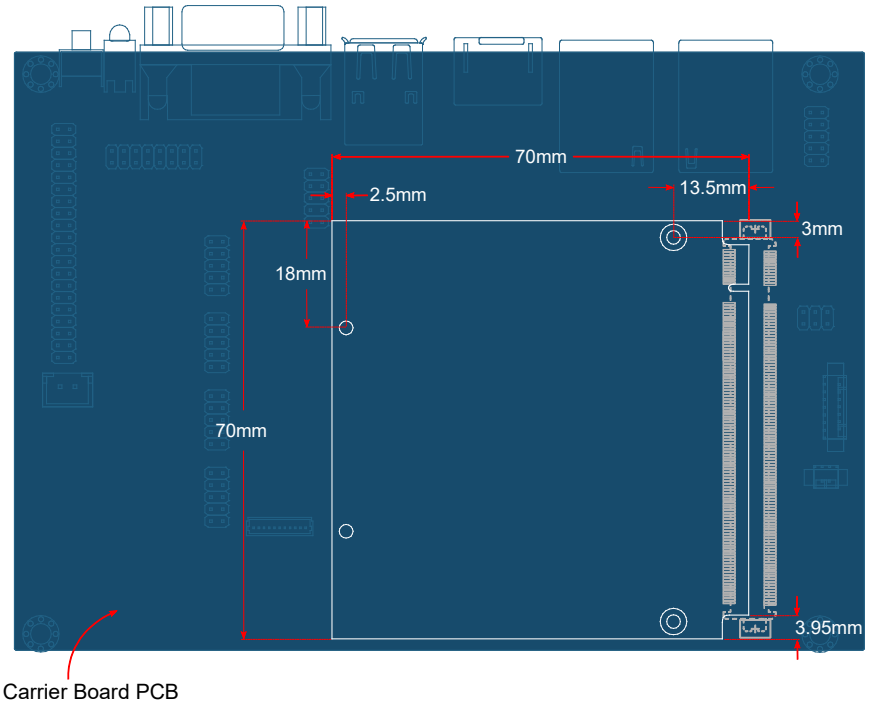

Figure 10: Qseven module placement on carrier board PCB

3.2. Qseven Mechanical Characteristics

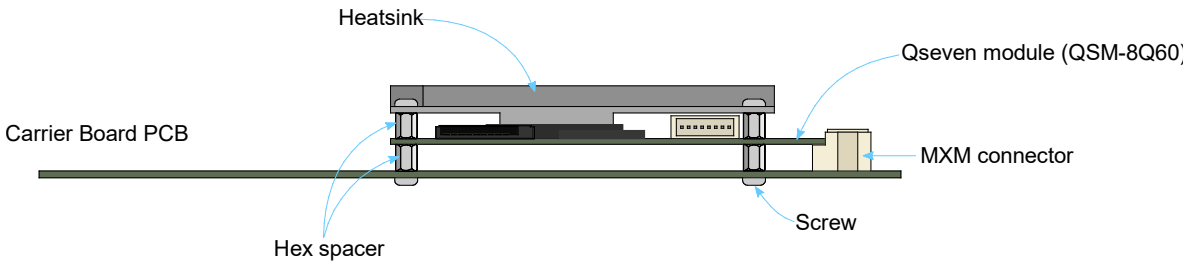

Figure 11: Carrier board with Qseven module installed

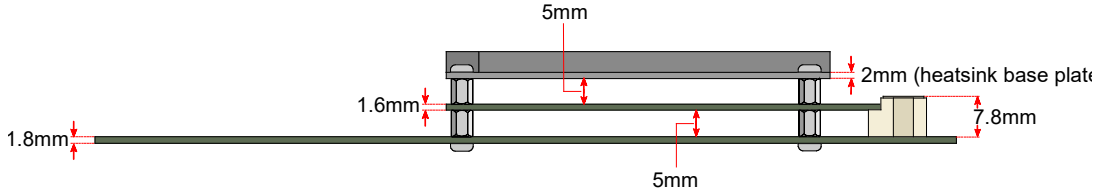

Figure 12: Qseven module and carrier board height distribution

3.3. VIA QSM-8Q60 Module and Carrier Board Dimensions

The mechanical dimensions of the QSM-Q860module and reference carrier board (QSMDB2) are shown below.

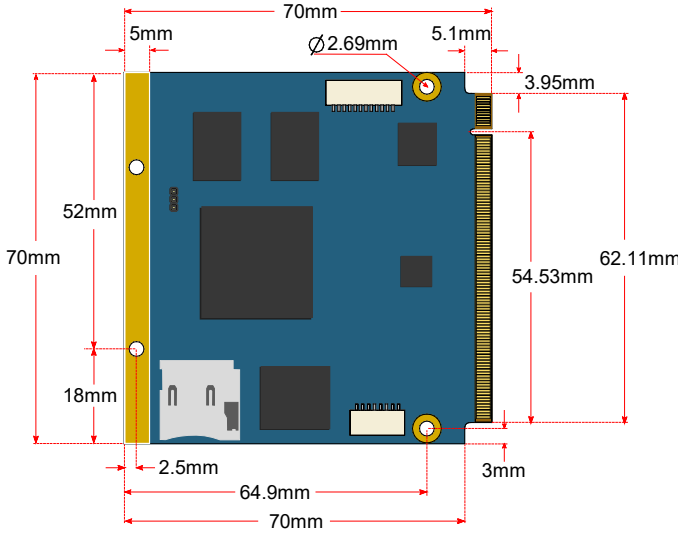

Figure 13: Dimensions of the VIA QSM-8Q60 module (top view)

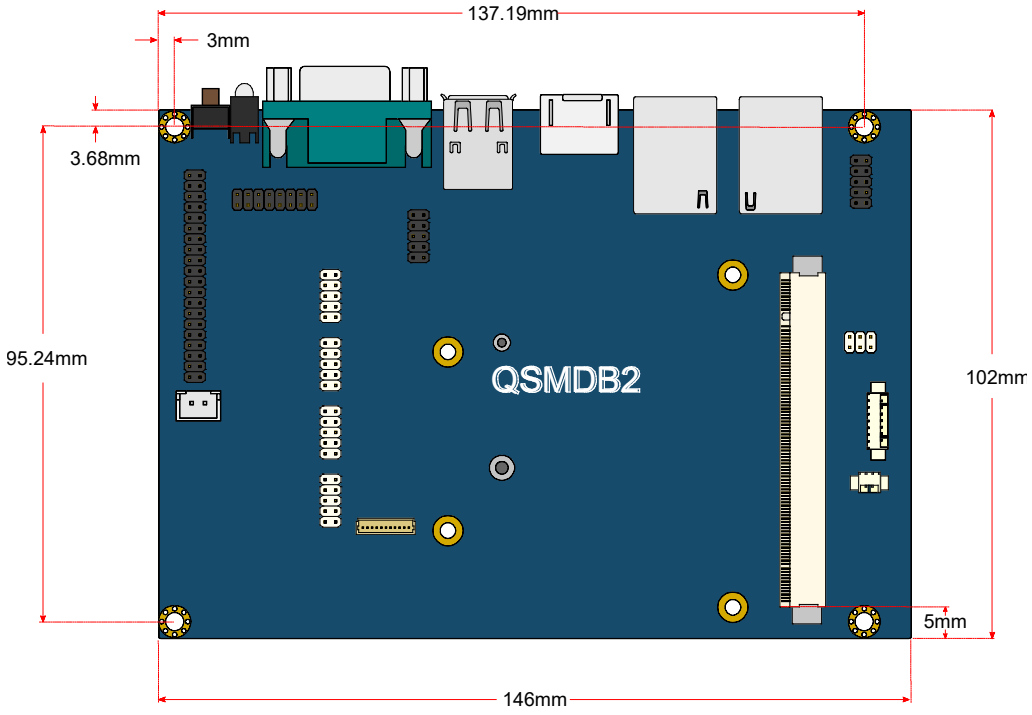

Figure 14: Dimensions of the carrier board (top view)

3.4. MXM Connector

The MXM connector can handle high-speed signals and comprises of 230-pins to connect the VIA QSM-8Q60 module.

Table 5 shows the specification of MXM connector with 7.8mm height.

Part Number	Resulting height between Qseven module and carrier board	Height	Vendor
AS0B326-S78N-7F	5mm	7.8mm	Foxconn

Table 5: MXM connector sample

3.4.1. MXM Connector Dimensions

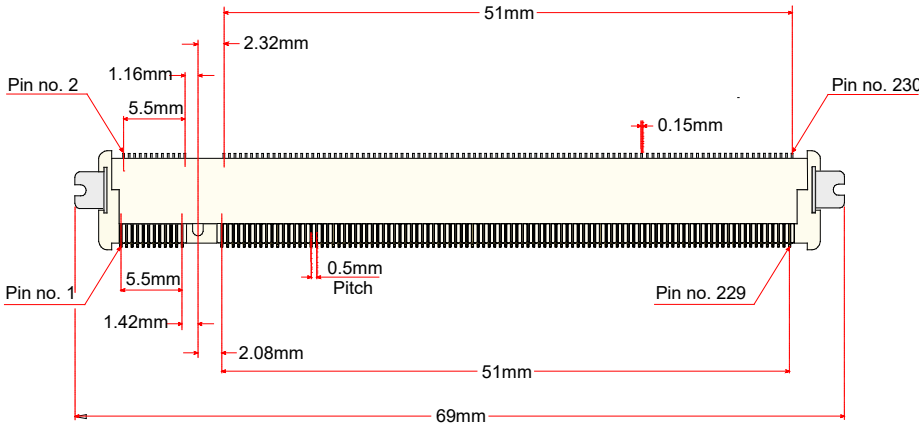

Figure 15: Dimensions of the MXM connector (top view)

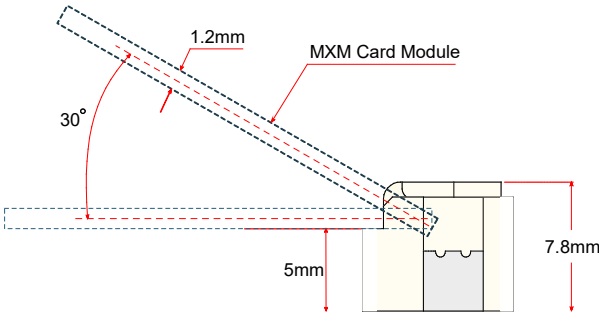

Figure 16: Dimensions of the MXM connector (side view)

3.4.2. MXM Connector Footprint

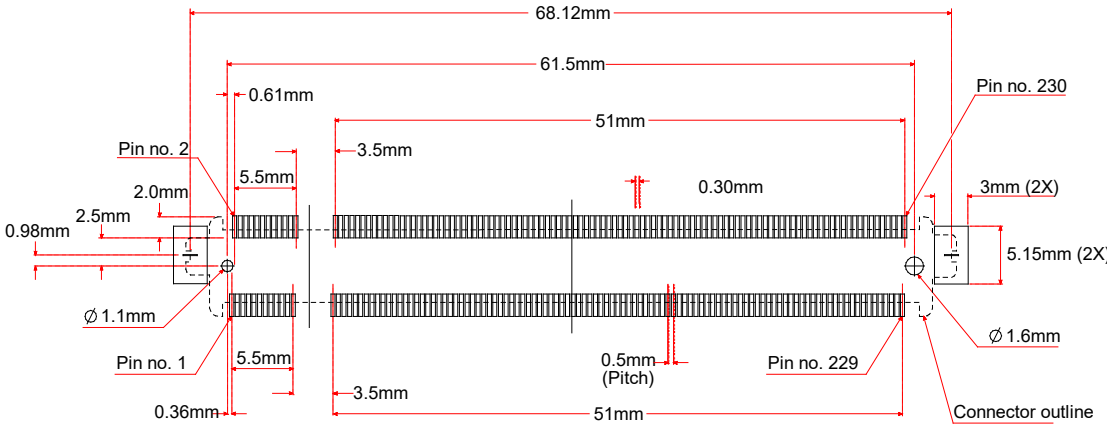

Figure 17: Carrier board PCB footprint for the MXM connector

3.4.3. VIA QSM-8Q60 Module and MXM Connector Footprint

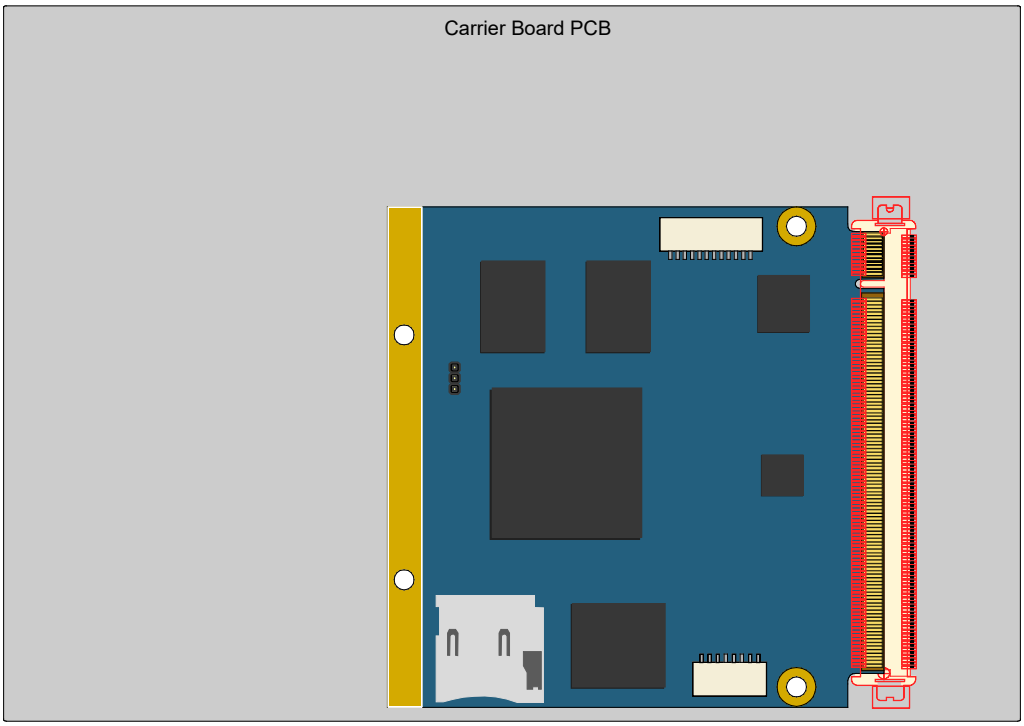

Figure 18: PCB footprint for Qseven module inserted in the MXM connector on the carrier board

3.5. MXM Connector Pinouts

The MXM connector is used for connecting the VIA QSM-8Q60 module to the Qseven carrier board. The MXM connector is consists of 230-pins. The pinout of the MXM connector is shown below.

Pin#	Pin Name	Signal	Pin#	Pin Name	Signal
1	GND	GND	2	GND	GND
3	GBE_MDI3-	TXRXM_D	4	GBE_MDI2-	TXRXM_C
5	GBE_MDI3+	TXRXP_D	6	GBE_MDI2+	TXRXP_C
7	GBE_LINK100-	NC	8	GBE_LINK1000-	NC
9	GBE_MDI1-	TXRXM_B	10	GBE_MDI0-	TXRXM_A
11	GBE_MDI1+	TXRXP_B	12	GBE_MDI0+	TXRXP_A
13	GBE_LINK#	LED2_LINK-	14	GBE_ACT#	LED1_ACT-
15	GBE_CTREF	NC	16	SUS_S5#	GPIO_19_PLED
17	WAKE-	NC	18	SUS_S3-	USB_OTG_PWR_EN
19	SUS_STAT-	NC	20	PWRBTN-	NC
21	SLP_BTN-	NC	22	LID_BTN-	NC
23	GND	GND	24	GND	GND
25	GND	GND	26	PWGIN	NC
27	BATLOW-	NC	28	RSTBTN#	RESET_N
29	SATA0_TX+	SATA0_TX+	30	SATA1_TX+	UART3_RX
31	SATA0_TX-	SATA0_TX-	32	SATA1_TX-	UART3_TX
33	SATA_ACT-	SATA_ACT-	34	GND	GND
35	SATA0_RX+	SATA0_RX+	36	SATA1_RX+	UART3_-CTS
37	SATA0_RX-	SATA0_RX-	38	SATA1_RX-	UART3_-RTS
39	GND	GND	40	GND	GND
41	BIOS_DISABLE-/BOOT_ALT-	NC	42	SDIO_CLK-	SD1_CLK
43	SDIO_CD-	SD1_CD-	44	SDIO_LED	SD1_LED
45	SDIO_CMD	SD1_CMD	46	SDIO_WP	SD1_WP
47	SDIO_PWR-	SD1_PWR-	48	SDIO_DATA1	SD1_DATA1
49	SDIO_DATA0	SD1_DATA0	50	SDIO_DATA3	SD1_DATA3
51	SDIO_DATA2	SD1_DATA2	52	SDIO_DATA5	SD1_DATA5
53	SDIO_DATA4	SD1_DATA4	54	SDIO_DATA7	SD1_DATA7
55	SDIO_DATA6	SD1_DATA6	56	RSVD	NC
57	GND	GND	58	GND	GND
59	HDA_SYNC /I2S_WS	AUD4_TXFS	60	SMB_CLK /GP1_I2C_CLK	UART2_RX
61	HDA_RST# /I2S_RST#	GPIO_0_CLKO	62	SMB_DAT /GP1_I2C_DAT	UART2_TX
63	HDA_BITCLK /I2S_CLK	AUD4_TXC	64	SMB_ALERT-	NC
65	HDA_SDI /I2S_SDI	AUD4_TXD	66	GP0_I2C_CLK	I2C3_SCL
67	HDA_SDO /I2S_SDO	AUD4_RXD	68	GP0_I2C_DAT	I2C3_SDA
69	THRM-	NC	70	WDTRIG-	NC
71	THRMTRIP-	NC	72	WDOUT	WDOG_B
73	GND	GND	74	GND	GND
75	USB_P7- /USB_SSTX0-	NC	76	USB_P6-/USB_SSRX0-	NC
77	USB_P7- /USB_SSTX0+	NC	78	USB_P6-/USB_SSRX0+	NC
79	USB_6_7_OC-	NC	80	USB_4_5_OC#	USB_4_OC

81	USB_P5- /USB_SSTX1-	NC	82	USB_P4-/USB_SSRX1-	USBD_T4-
83	USB_P5- /USB_SSTX1+	NC	84	USB_P4-/USB_SSRX1+	USBD_T4+
85	USB_2_3_OC#	USB_2_3_OC	86	USB_0_1_OC#	USB_0_OTG_OC
87	USB_P3-	USBD_T3-	88	USB_P2-	USBD_T2-
89	USB_P3+	USBD_T3+	90	USB_P2+	USBD_T2+
91	USB_CC	NC	92	USB_ID	USBD_OTG_ID
93	USB_P1-	OTG_USBD_T1-	94	USB_P0-	USBD_T0-
95	USB_P1+	OTG_USBD_T1+	96	USB_P0+	USBD_T0+
97	GND	GND	98	GND	GND
99	eDP0_TX0+ /LVDS_A0+	LVDS0_TX0_P	100	eDP1_TX0+ /LVDS_B0+	LVDS1_TX0_P
101	eDP0_TX0- /LVDS_A0-	LVDS0_TX0_N	102	eDP1_TX0- /LVDS_B0-	LVDS1_TX0_N
103	eDP0_TX1+ /LVDS_A1+	LVDS0_TX1_P	104	eDP1_TX1+ /LVDS_B1+	LVDS1_TX1_P
105	eDP0_TX1- /LVDS_A1-	LVDS0_TX1_N	106	eDP1_TX1- /LVDS_B1-	LVDS1_TX1_N
107	eDP0_TX2+ /LVDS_A2+	LVDS0_TX2_P	108	eDP1_TX2+ /LVDS_B2+	LVDS1_TX2_P
109	eDP0_TX2- /LVDS_A2-	LVDS0_TX2_N	110	eDP1_TX2- /LVDS_B2-	LVDS1_TX2_N
111	LVDS_PPEN	LVDS_PPEN	112	LVDS_BLEN	LVDS_BLEN
113	eDP0_TX3+ /LVDS_A3+	LVDS0_TX3_P	114	eDP1_TX3+ /LVDS_B3+	LVDS1_TX3_P
115	eDP0_TX3- /LVDS_A3-	LVDS0_TX3_N	116	eDP1_TX3- /LVDS_B3-	LVDS1_TX3_N
117	GND	GND	118	GND	GND
119	eDP0_AUX+ /LVDS_A_CLK+	LVDS0_CLK_P	120	eDP1_AUX+ /LVDS_B_CLK+	LVDS1_CLK_P
121	eDP0_AUX- /LVDS_A_CLK-	LVDS0_CLK_N	122	eDP1_AUX- /LVDS_B_CLK-	LVDS1_CLK_N
123	LVDS_BLT_CTRL /GP_PWM_OUT0	LVDS_PWM2	124	GP_1-Wire_Bus	NC
125	GP2_I2C_DAT /LVDS_DID_DAT	I2C1_SDA	126	eDP0_HPD# /LVDS_BLC_DAT	USB_0_2_3_4_EN
127	GP2_I2C_CLK /LVDS_DID_CLK	I2C1_SCL	128	eDP1_HPD# /LVDS_BLC_CLK	HDMI_CEC_IN
129	CAN0_TX	CAN_TX1	130	CAN0_RX	CAN_RX1
131	DP_LANE3+ /TMDS_CLK+	HDMI_CLKP	132	RSVD(Differential)	TP_2
133	DP_LANE3- /TMDS_CLK-	HDMI_CLKM	134	RSVD(Differential)	TP_3
135	GND	GND	136	GND	GND
137	DP_LANE1+ /TMDS_LANE1+	HDMI_D1P	138	DP_AUX+	NC
139	DP_LANE1- /TMDS_LANE1-	HDMI_D1M	140	DP_AUX-	NC
141	GND	GND	142	GND	GND
143	DP_LANE2+ /TMDS_LANE0+	HDMI_D0P	144	RSVD(Differential)	NC
145	DP_LANE2- /TMDS_LANE0-	HDMI_D0M	146	RSVD(Differential)	NC
147	GND	GND	148	GND	GND

149	DP_LANE0+ /TMDS_LANE2+	HDMI_D2P	150	HDMI_CTRL_DAT	I2C2_SDA
151	DP_LANE0- /TMDS_LANE2-	HDMI_D2M	152	HDMI_CTRL_CLK	I2C2_SCL
153	DP_HDMI_HPD#	HDMI_HPD	154	RSVD	GND
155	PCIE_CLK_REF+	PCIe_CREFCLKP	156	PCIE_WAKE#	PCIE_WAKE_B
157	PCIE_CLK_REF-	PCIe_CREFCLKM	158	PCIE_RST#	PCIE_RST_B
159	GND	GND	160	GND	GND
161	PCIE3_TX+	NC	162	PCIE3_RX+	NC
163	PCIE3_TX-	NC	164	PCIE3_RX-	NC
165	GND	GND	166	GND	GND
167	PCIE2_TX+	NC	168	PCIE2_RX+	NC
169	PCIE2_TX-	NC	170	PCIE2_RX-	NC
171	UART0_TX	UART1_TX	172	UART_RTS-	UART1_-RTS
173	PCIE1_TX+	NC	174	PCIE1_RX+	CAN_TX2
175	PCIE1_TX-	NC	176	PCIE1_RX-	CAN_RX2
177	UART0_RX	UART1_RX	178	UART0_CTS	UART1_CTS
179	PCIE0_TX+	PCIe_CTXP	180	PCIE0_RX+	PCIe_CRXP
181	PCIE0_TX-	PCIe_CTXM	182	PCIE0_RX-	PCIe_CRXM
183	GND	GND	184	GND	GND
185	LPC_AD0/GPIO0	GPIO6_IO11	186	LPC_AD1/GPIO1	TP_6
187	LPC_AD2/GPIO2	GPIO_2	188	LPC_AD3/GPIO3	TP_7
189	LPC_CLK/GPIO4	GPIO6_IO14	190	LPC_FRAME#/GPIO5	TP_8
191	SERIRQ/GPIO6	GPIO_5	192	LPC_LDRQ#/GPIO7	TP_9
193	VCC_RTC	VDD_RTC_IN	194	SPKR/GP_PWM_OUT2	NC
195	FAN_TACHOIN /GP_TIMER_IN	NC	196	FAN_PWM /GP_PWM_OUT1	PWM_OUT1
197	GND	GND	198	GND	GND
199	SPI_MOSI	CSPI3_MOSI	200	SPI_CS0#	CSPI3_CS0
201	SPI_MISO	CSPI3_MISO	202	SPI_CS1#	CSPI3_CS1
203	SPI_SCK	CSPI3_CLK	204	MFG_NC4	NC
205	VCC_5V_SB	NC	206	VCC_5V_SB	NC
207	MFG_NC0	NC	208	MFG_NC2	NC
209	MFG_NC1	NC	210	MFG_NC3	NC
211	VCC	5VIN	212	VCC	5VIN
213	VCC	5VIN	214	VCC	5VIN
215	VCC	5VIN	216	VCC	5VIN
217	VCC	5VIN	218	VCC	5VIN
219	VCC	5VIN	220	VCC	5VIN
221	VCC	5VIN	222	VCC	5VIN
223	VCC	5VIN	224	VCC	5VIN
225	VCC	5VIN	226	VCC	5VIN
227	VCC	5VIN	228	VCC	5VIN
229	VCC	5VIN	230	VCC	5VIN

Table 6: MXM connector pinout

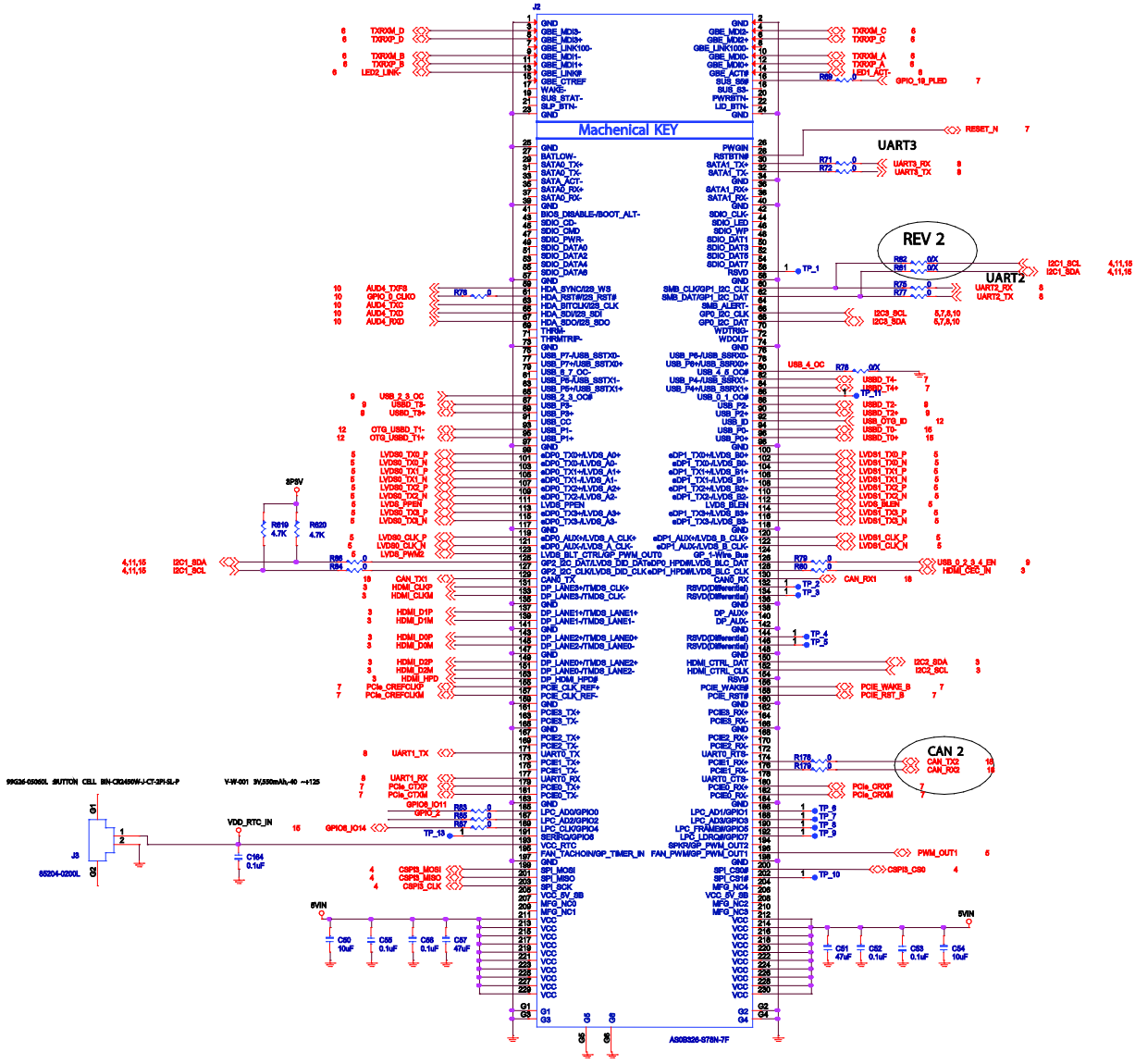

Figure 19: MXM connector schematics

4. Layout and Routing Recommendations

The information presented in this chapter includes the signal descriptions, reference schematic examples, topology examples, and detailed layout and routing guidelines for each bus interface. The information provided is intended for designing the Qseven compliant carrier boards to support the features of VIA QSM-8Q60 module.

4.1. PCI Express Interface

This section will guide the developer to create a robust PCI Express interface design in the Qseven carrier board. However, the carrier board designer should do an appropriate analysis and simulation to verify that the design fulfills PCI Express specification requirements.

The PCI Express is a serial differential low-voltage, point-to-point interface. A PCI Express consists of two differential signal pairs (for transmit data pair and receive data pair), and one pair for reference clock. The bandwidth of a PCI Express link can be increased by adding signal pairs to form multiple lanes between two devices.

The VIA QSM-8Q60 module can support one PCI Express x1 through miniPCIe slot.

Signal Name	Pin #	I/O	Description
PCIE0_RX+	180	IO	Receive input differential pair, PCIe channel 0.
PCIE0_RX-	182		
PCIE0_TX+	179	IO	Transmit output differential pair, PCIe channel 0.
PCIE0_TX-	181		
PCIE_CLK_REF+	155	IO	PCIe reference clock for Lane 0.
PCIE_CLK_REF-	157		
PCIE_WAKE#	156	IO	PCIe wake event up signal: Sideband wake signal asserted by components requesting wakeup.
PCIE_RST#	158	IO	Reset signal for external devices.

Table 7: PCI Express signal group and definition

4.1.1. MiniPCIe Slot

The miniPCIe slot consists of a single PCI Express x1.The miniPCIe slot is a 52-pin connector designed for add-in PCI Express Mini Cards. Applying the miniPCIe slot on the carrier board will provide the ability to insert different removable and upgradeable miniPCIe cards without the additional expenditure to redesign the carrier board.

Pin	Signal	Description
1	PCIE_WAKE_B	Request to return to full operation and respond to PCIe
2	MPCIE_3V3	Primary source voltage, 3.3V
3	NC	No Connection/Reserved
4	GND	Ground
5	NC	No Connection/Reserved
6	DDR_1_5V	Secondary source voltage, 1.5V
7	NC	No Connection/Reserved
8	USIM_VCC	Power source for User Identity Modules
9	GND	Ground
10	USIM_DATA	Data signal for User Identity Module
11	PCIe_CREFCLKM	Negative reference clock differential pair
12	USIM_CLK	Clock signal for User Identity Module
13	PCIe_CREFCLKP	Positive reference clock differential pair
14	USIM_RST	Reset signal for User Identity Module
15	GND	Ground
16	USIM_VCC	Variable supply voltage for User Identity Module
17	NC	No Connection/Reserved

18	GND	Ground
19	NC	No Connection/Reserved
20	NC	No Connection/Reserved
21	GND	Ground
22	PCIE_RST_B	PCI Express reset
23	PCIe_CRXM	Receiver differential pair negative signal, Lane 0
24	MPCIE_3V3	Auxiliary voltage source, 3.3V
25	PCIe_CRXP	Receiver differential pair positive signal, Lane 0
26	GND	Ground
27	GND	Ground
28	DDR_1_5V	Secondary source voltage, 1.5V
29	GND	Ground
30	PCIe_SMB_CLK	System Management Bus clock
31	PCIe_CTXM	Transmit differential pair negative signal, Lane 0
32	PCIe_SMB_DATA	System Management Bus data
33	PCIe_CTXP	Transmit differential pair positive signal, Lane 0
34	GND	Ground
35	GND	Ground
36	PCIE_USB_DM	USB data interface differential pair, negative signal
37	GND	Ground
38	PCIE_USB_DP	USB data interface differential pair, positive signal
39	MPCIE_3V3	Primary source voltage, 3.3V
40	GND	Ground
41	MPCIE_3V3	Primary source voltage, 3.3V
42	LED_WWAN_B	LED status indicator signal
43	GND	Ground
44	LED_WLAN_B	LED status indicator signal
45	NC	No Connection/Reserved
46	LED_WPAN_B	LED status indicator signal
47	NC	No Connection/Reserved
48	DDR_1_5V	Secondary source voltage, 1.5V
49	NC	No Connection/Reserved
50	GND	Ground
51	NC	No Connection/Reserved
52	MPCIE_3V3	Primary source voltage, 3.3V

Table 8: MiniPCIe slot pinout definition

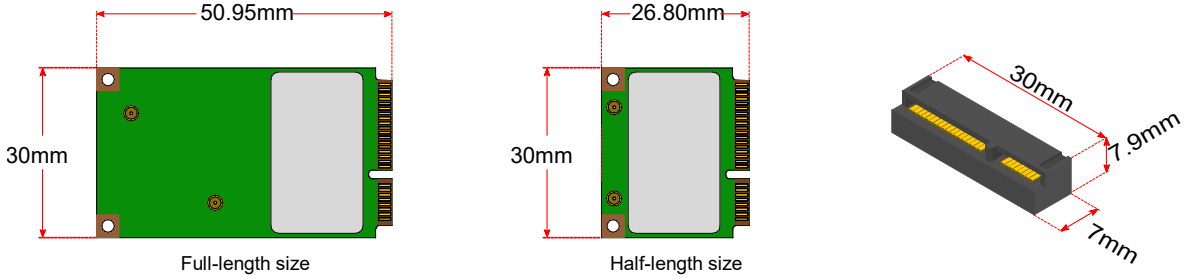

Figure 20: MiniPCIe card and slot diagram

The PCI Express signal has a point-to-point topology. The figure below shows the PCI Express x1 point-to-point bus connection from MXM connector to MiniPCI Express slot/device.

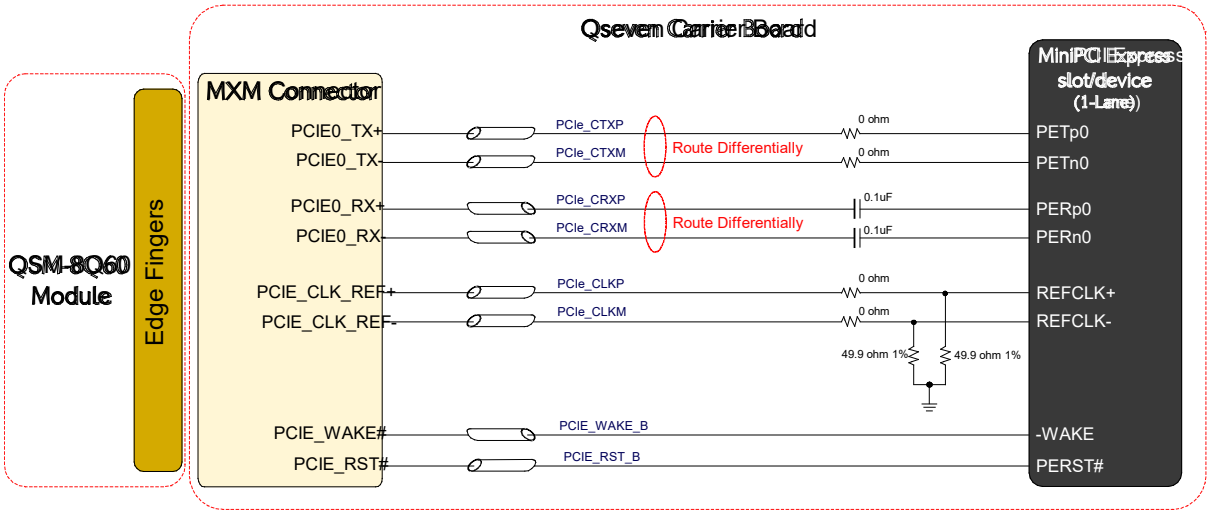

Figure 21: MiniPCI Express interface topology example

4.1.2. PCI Express Layout and Routing Recommendations

- All the PCI Express signals should be referenced to the ground plane at all times.
- Each trace of differential pairs should route to parallel to each other with the same trace length.
- Each trace of differential pairs should not have more than two via holes.
- Place the AC coupling capacitors as close as possible to the PCI Express slot/device.
- The spacing between differential pairs must be equal at all times (in parallel), even during trace bending and serpentine topology.
- Differential pairs must be routed on the same layer with maximum of one signal layer change allowed. The differential pairs must always move to the same layer with the same reference plane.
- Transmit differential pairs are recommended to be routed on the top layer and receive differential pairs are recommended to be routed on the bottom layer.
- Do not route PCI Express traces under magnetic devices or IC's, oscillators and clock synthesizers.
- To minimize signal crosstalk, wider spacing is recommended wherever possible between traces.
- It is always best to reduce the line mismatch to add to the timing margin. In other words, a balanced topology can match the trace lengths within the groups to minimize skew.

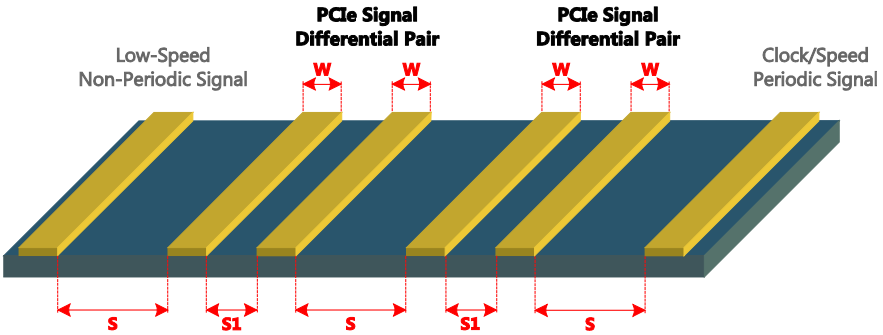

Figure 22: PCI Express trace spacing diagram

Routing, layout, and trace properties for implementing PCI Express interface in the carrier board are listed in the following tables.

Signal Group		Signal Name	AC Coupling Capacitors	Routing Topology	Signal Type
1-Lane PCI Express	Transmit	PCIE0_TX+	None	Point to Point	Paired Differential Transmit/Receive Signals
		PCIE0_TX-	None		
	Receive	PCIE0_RX+	0.1uF		
		PCIE0_RX-	0.1uF		

Table 9: PCI Express interface routing guidelines

Signal Group		Signal Name	Routing Layer	Accumulated Trace Length	Note
1-Lane PCI Express	Transmit	PCIE0_TX+	Top or Bottom	< 2.6"	Do not cross power plane division line
		PCIE0_TX-			
	Receive	PCIE0_RX+	Top or Bottom	< 2.6"	
		PCIE0_RX-			

Table 10: PCI Express interface layout guidelines

Signal Name	Trace & Spacing (mil) (S : W : S1 : W : S)	Differential Trace Impedance	Pair to Pair Length Mismatch	Spacing to Other Groups
PCIE0_TX+	20 : 5 : 5 : 5 : 20	85Ω ± 15%	5 mils	20 mils
PCIE0_TX-				
PCIE0_RX+				
PCIE0_RX-				

Table 11: PCI Express interface trace properties

4.1.3. PCI Express Reference Schematics

The figure below show an example on how a miniPCIe slot can be connected to a Qseven carrier board.

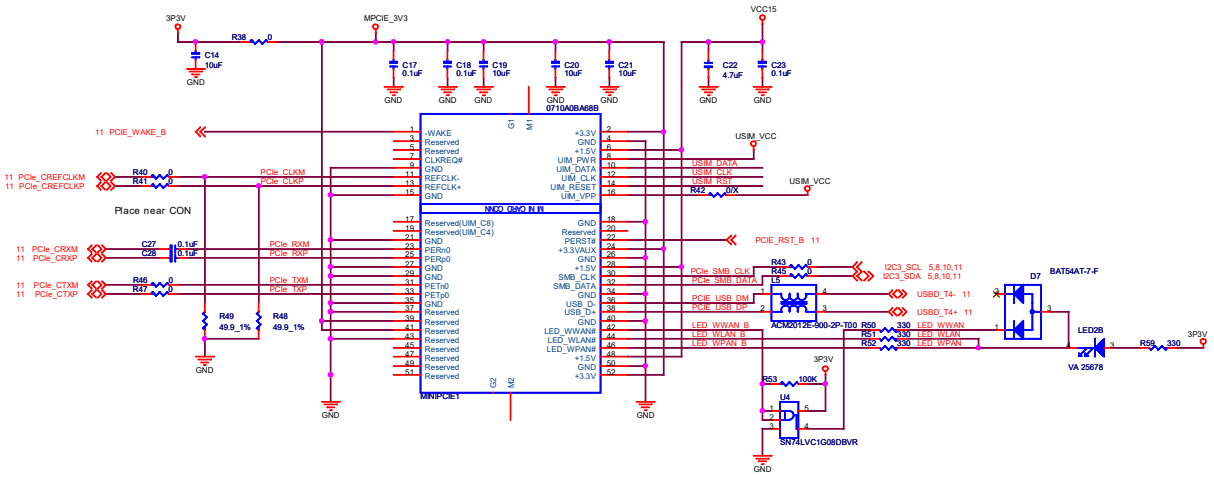

Figure 23: MiniPCIe slot reference circuitry

4.2. Ethernet Interface

The VIA QSM-8Q60 module provides one Gigabit Ethernet (LAN) port that complies with the IEEE standard for 10BASE-T, 100BASE-T, 1000BASE-T, TX and T4 Ethernet interfaces.

The Gigabit Ethernet (LAN) interface of the VIA QSM-8Q60 module consists of four differential signals and control signals for activity link indicators. These signals can be used to connect to the RJ-45 port with integrated or external isolation magnetic (transformer) to the carrier board.

Signal Name	Pin #	I/O	Description
GBE_MDI0+	12	IO	Media Dependent Interface differential pair 0. The TXRX can operate in 1000, 100, and 10Mbps modes. This signal pair is used for all modes.
GBE_MDI0-	10		
GBE_MDI1+	11	IO	Media Dependent Interface differential pair 1. The TXRX can operate in 1000, 100, and 10Mbps modes. This signal pair is used for all modes.
GBE_MDI1-	9		
GBE_MDI2+	6	IO	Media Dependent Interface differential pair 2. The TXRX can operate in 1000, 100, and 10Mbps modes. This signal pair is only used 1000Mbps Gigabit Ethernet mode.
GBE_MDI2-	4		
GBE_MDI3+	5	IO	Media Dependent Interface differential pair 3. The TXRX can operate in 1000, 100, and 10Mbps modes. This signal pair is only used 1000Mbps Gigabit Ethernet mode.
GBE_MDI3-	3		
GBE_LINK#	13	IO	Ethernet controller link indicator, active low
GBE_ACT#	14	IO	Ethernet controller 0 activity indicator

Table 12: Ethernet signal definition

4.2.1. Ethernet Interface Topology

This section shows the layout recommendations of both transmit and receive differential data pairs and single-ended control signal between the VIA QSM-8Q60 module and RJ-45 port with integrated magnetic module.

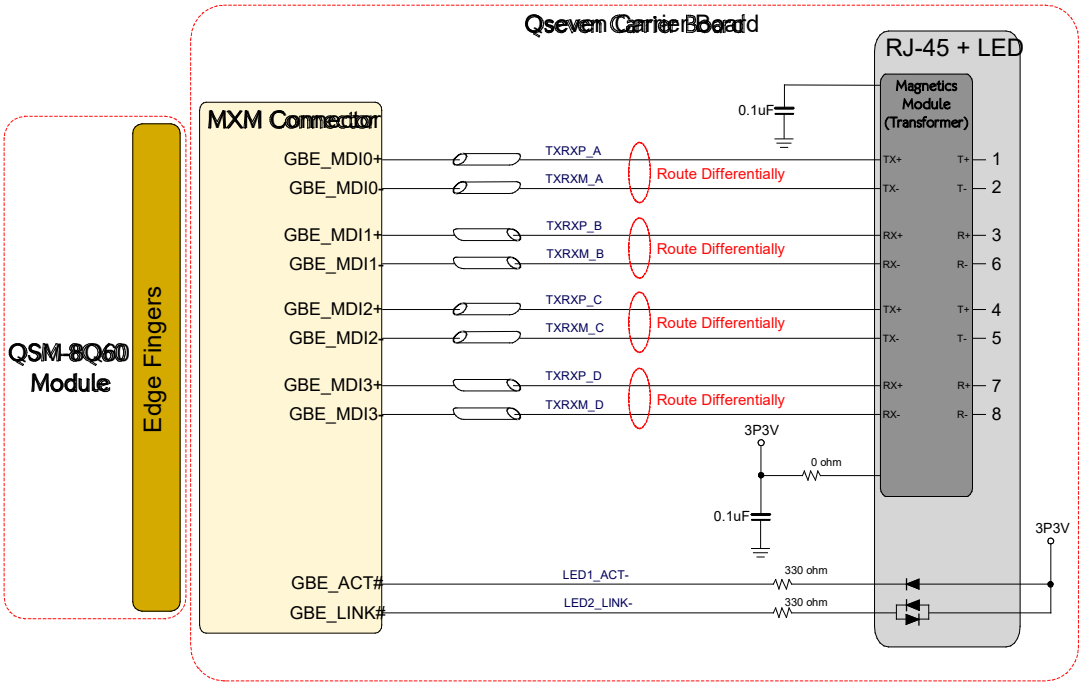

Figure 24: Gigabit Ethernet layout recommendations (integrated magnetic module)

Notes:

1. If the Gigabit Ethernet implementation is not being use, the pins GBE_MDI2+, GBE_MDI2-, GBE_MDI3+ and GBE_MDI3- should not be connected.
2. It is recommended to use termination circuits for the unused pin at the RJ-45 connector and for wire-side center-taps of the magnetic module. Improper usage (or lack of usage) of the termination circuits for those unused pins at the RJ-45 connector wire-side center taps of the transformer will cause emissions and long cable noise problems related to other IEEE conformance issues.
3. If using an external LAN magnetic module, the magnetic module has to be placed as close as possible to the RJ-45 port. The distance must be <1".

4.2.2. Gigabit Ethernet Layout and Routing Recommendations

- Route differential pairs close together and away from other signals.
- Route any other trace parallel to one of the differential trace.
- Keep trace length within each differential pair equal.
- Keep proper impedance between two traces within a differential pair.
- Each trace of differential pairs should not have more than two via holes.
- Each differential pair of signals is required to be paralleled to each other with the same trace length (Tolerance ±50 mils) on the component (top) layer and to be paralleled to a respective ground plane. The length difference between the shortest and longest pairs should be less than 200 mils.
- The accumulated trace length of differential signals pair between the MXM connector and magnetic module should be less than 1".
- The accumulated trace length of differential signals pair between the external magnetic module and RJ-45 connector should be less than 1". Isolate ground plane and connect to chassis earth.
- Keep each differential pair on the same plane.
- To prevent any noise from injecting into the differential pairs, be sure to keep digital signals or other signals away from the differential signals.
- The external magnetic module should be placed close to the RJ-45 connector to limit EMI emissions.

Routing, layout, and trace properties for implementing Gigabit Ethernet interface in the carrier board are listed in the following tables.

Signal Group	Signal Name	Topology	Signal Type	Note
Differential Pair	GBE_MDI0+	Point to Point	Differential Data I/O Pairs	Route traces as short as possible
	GBE_MDI0-			
	GBE_MDI1+			
	GBE_MDI1-			
	GBE_MDI2+			
	GBE_MDI2-			
	GBE_MDI3+			
	GBE_MDI3-			
Control	GBE_LINK#	Point to Point	Single-Ended	Route traces as short as possible
	GBE_ACT#			

Table 13: Gigabit Ethernet interface routing guidelines

Signal Group	Signal Name	Routing Layer	Accumulated Trace Length	Note
Differential Pair	GBE_MDI0+	Top Layer	< 1.2"	Do not cross power plane division line
	GBE_MDI0-			
	GBE_MDI1+			
	GBE_MDI1-			
	GBE_MDI2+			
	GBE_MDI2-			
	GBE_MDI3+			
	GBE_MDI3-			
Control	GBE_LINK#	Top Layer	< 1.2"	Do not cross power plane division line
	GBE_ACT#			

Table 14: Gigabit Ethernet interface layout guidelines

Signal Name	Trace & Spacing (mil) (S : W : S1 : W : S)	Trace Impedance	Pair to Pair Length Mismatch	Spacing to Other Group
GBE_MDI0+	20 : 5 : 8 : 5 : 20	100Ω ± 15% differential	5 mils	20 mils
GBE_MDI0-				
GBE_MDI1+				
GBE_MDI1-				
GBE_MDI2+				
GBE_MDI2-				
GBE_MDI3+				
GBE_MDI3-				
GBE_LINK#	5 : 8	55Ω ± 10%	-	20 mils
GBE_ACT#				

Table 15: Gigabit Ethernet interface trace properties

4.2.3. Gigabit Ethernet Reference Schematics

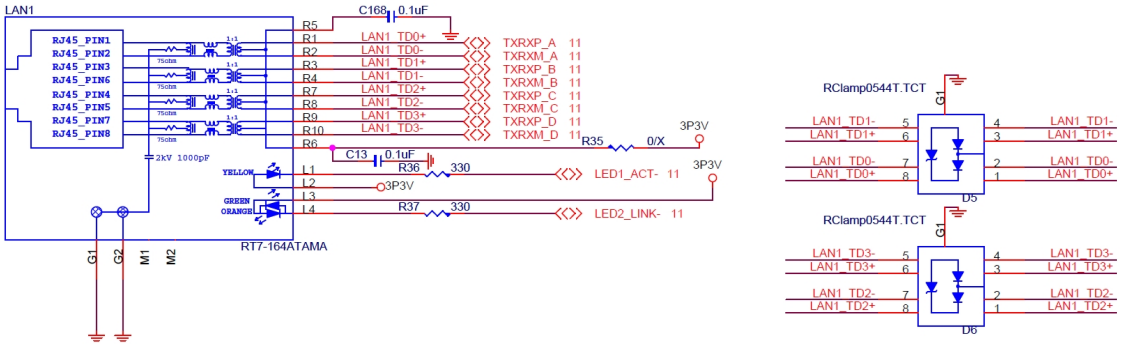

Figure 25: Gigabit Ethernet reference circuitry

4.3. USB Interface

The Universal Serial Bus (USB) provides a bi-directional, isochronous, hot-attachable Plug and Play serial interface for adding external peripheral devices (e.g., game controllers, communication devices, and input devices) on a single bus. The USB interface of the VIA QSM-8Q60 module is compliant to USB 2.0 specification.

The VIA QSM-8Q60 module can support up to four USB 2.0 host and one USB 2.0 client port.

Signal Name	Pin #	I/O	Description
USB_P0+	96	IO	Universal Serial Bus port 0, data+
USB_P0-	94	IO	Universal Serial Bus port 0, data-
USB_P1+	95	IO	OTG Universal Serial Bus port 1, data+
USB_P1-	93	IO	OTG Universal Serial Bus port 1, data-
USB_P2+	90	IO	Universal Serial Bus port 2, data+
USB_P2-	88	IO	Universal Serial Bus port 2, data-
USB_P3+	89	IO	Universal Serial Bus port 3, data+
USB_P3-	87	IO	Universal Serial Bus port 3, data-
USB_P4+	84	IO	Universal Serial Bus port 4, data+
USB_P4-	82	IO	Universal Serial Bus port 4, data-
USB_2_3_OC#	85	I	Universal Serial Bus over-current sense, USB ports 2 and 3
USB_4_5_OC#	80	I	Universal Serial Bus over-current sense, USB port 4
USB_ID	92	I	Universal Serial Bus I.D. pin. Configures the mode of USB port 1

Table 16: USB signal definition

4.3.1. USB Layout and Routing Recommendations

- The layout guidelines for the USB data lines are listed below. And a routing example for two pairs of USB data buses is shown in Figure 27.
- The differential pair signals should be all referenced to ground.
- Each trace of differential pairs should not have more than two via holes.
- Differential pair route in parallel and in equal length.
- The amount of vias and corners used for the USB 2.0 signal layout should be minimized; this is to prevent the occurrence of reflection and impedance changes.
- Each pair of USB data lines is required to be parallel to each other with the same trace length (see Figure 27), and not parallel with other signals to minimize crosstalk.
- Separate the signal traces into similar groups and route similar signal traces together. In addition, it is recommended to have differential pairs routed together on the motherboard.
- Control trace signals (USB_2_3_OC#, USB_4_5_OC# and USB_ID) impedance should maintain 55Ω ± 10%.
- For the USB traces, do not route them under oscillators, crystals, clock synthesizers, magnetic devices or IC's which could be using duplicate clocks.

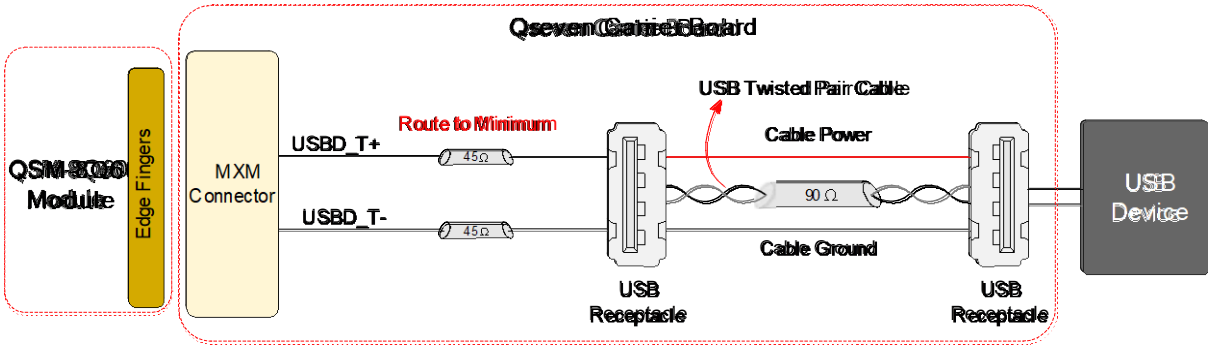

Figure 26: USB differential signal layout recommendations

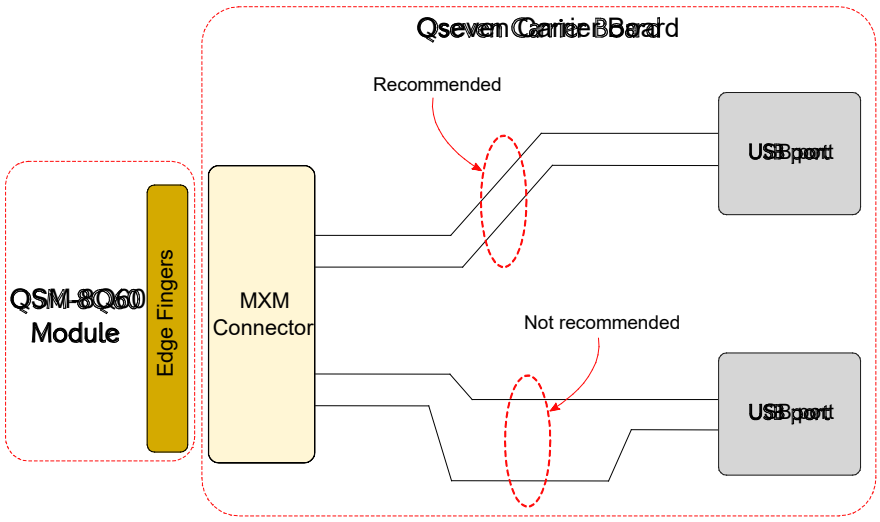

Figure 27: USB differential signal routing example

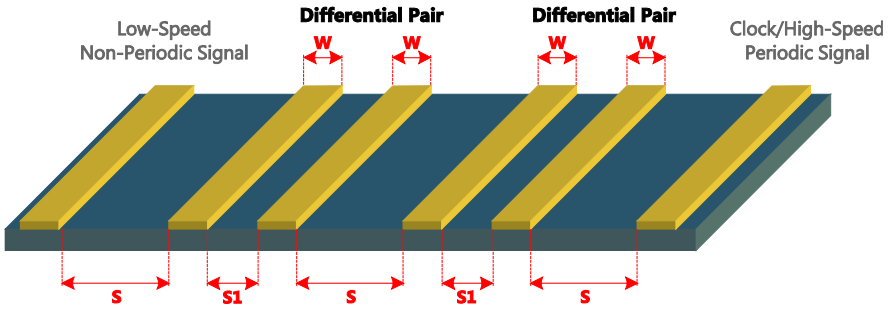

Figure 28: USB 2.0 trace spacing diagram

Routing, layout, and trace properties for implementing USB interface in the carrier board are listed in the following tables.

Signal Group		Signal Name	Termination Option	Topology	Signal Type
Differential Data Pair	Port 0	USB_P0+	None	Point-to-Point	Differential Data I/O Pairs
		USB_P0-			
	Port 1	USB_P1+			
		USB_P1-			
	Port 2	USB_P2+			
		USB_P2-			
	Port 3	USB_P3+			
		USB_P3-			
	Port 4	USB_P4+			
		USB_P4-			
Control		USB_2_3_OC#	None	Point-to-Point	Single-ended
		USB_4_5_OC#			
		USB _ID			

Table 17: USB interface routing guidelines

Signal Group		Signal Name	Routing Layer	Termination Stub Length	Accumulated Trace Length	Note
Differential Data Pair	Port 0	USB_P0+	Top or Bottom	< 1″	< 4″	
		USB_P0-				
	Port 1	USB_P1+				
		USB_P1-				
	Port 2	USB_P2+				
		USB_P2-				
	Port 3	USB_P3+				
		USB_P3-				
	Port 4	USB_P4+				
		USB_P4-				
Control	USB_2_3_OC#		Top or Bottom	< 1″	Route to minimum	
	USB_4_5_OC#					
	USB_ID					

Table 18: USB interface layout guidelines

Signal Name	Trace Impedance	Trace & Spacing (mil) (S : W : S1 : W : S)	Pair to Pair Length Mismatch	Spacing to Other Group
USB_P0+	90Ω ± 15%	20 : 5 : 5 : 5 : 20	5 mils	< 0.03″
USB_P0-				
USB_P1+				
USB_P1-				
USB_P2+				
USB_P2-				
USB_P3+				
USB_P3-				
USB_P4+				
USB_P4-				
USB_2_3_OC#	55Ω ± 10	5 : 10	-	< 0.02″
USB_4_5_OC#				
USB_ID				

Table 19: USB interface trace properties

4.3.2. USB Reference Schematics

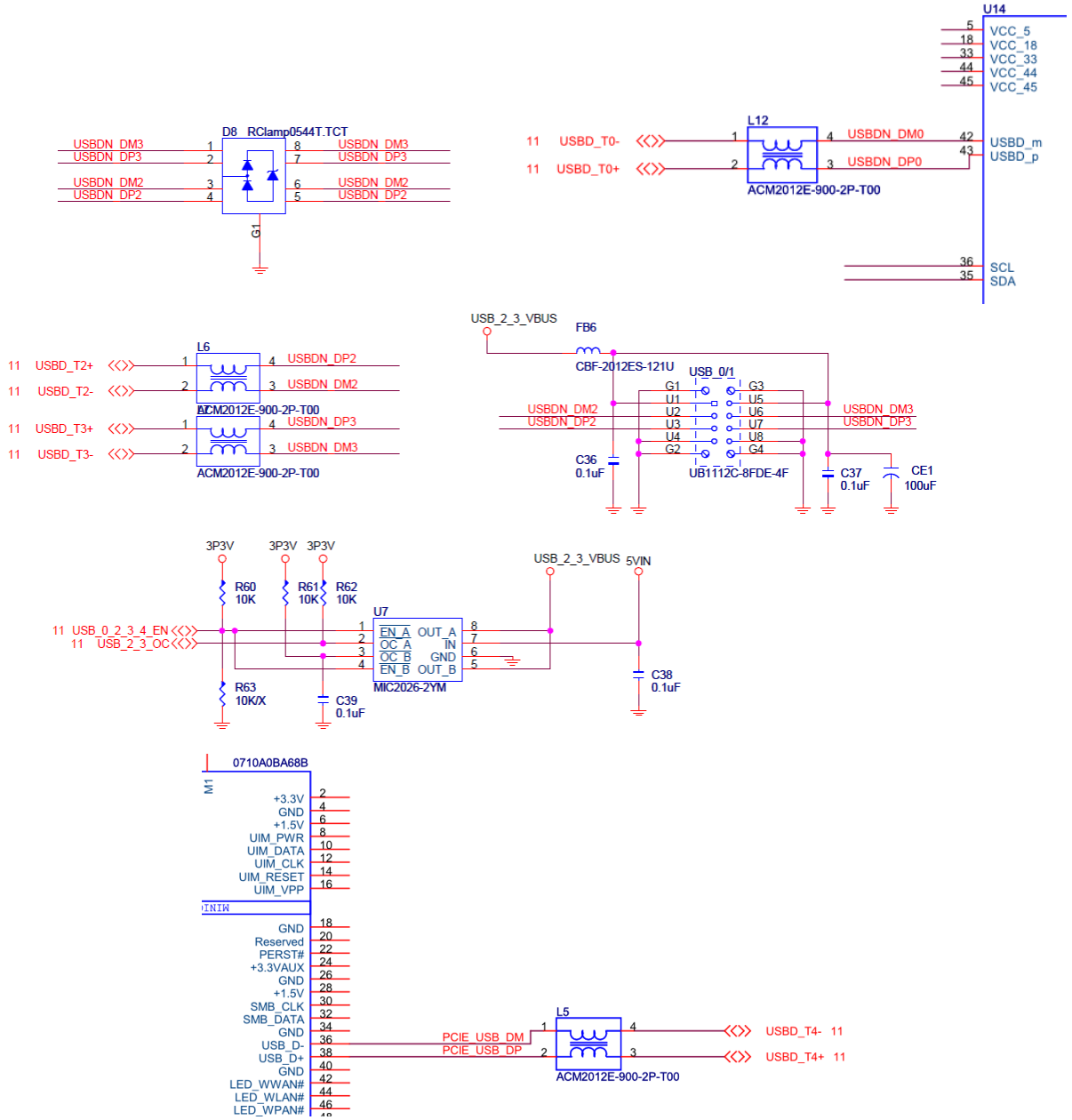

Figure 29: USB host reference circuitry

The USB port mode can be controlled by the signal USB_ID. In the reference circuitry example below, the USB_ID signal is referenced to ground that makes the USB port 1 mode as Client USB (or USB OTG port).

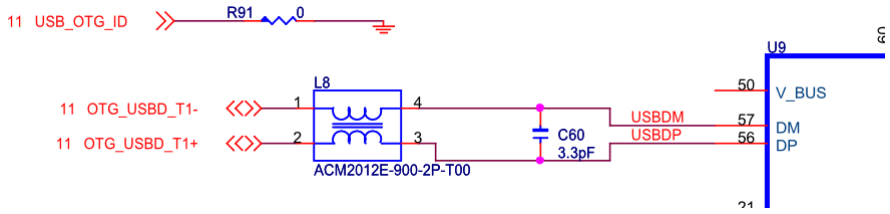

Figure 30: USB client reference circuitry

4.4. LVDS Interface

The LVDS interface in the VIA QSM-8Q60 module enables displaying graphics on LVDS flat panel. The LVDS is a dual-channel that supports 18-bit and 24-bit interfaces.

The LVDS signal interface consists of four differential data pairs and one differential clock pair for each channel, and five single-ended control signals. The five single-ended control signals are used for LVDS power enable, backlight control, enable lines and I^2C interface.

The LVDS interface signals are implemented in MXM connector.

Signal Name	Pin #	I/O	Description
LVDS_A0+	99	O	LVDS channel A differential signal pair 0
LVDS_A0-	101		
LVDS_A1+	103	O	LVDS channel A differential signal pair 1
LVDS_A1-	105		
LVDS_A2+	107	O	LVDS channel A differential signal pair 2
LVDS_A2-	109		
LVDS_A3+	113	O	LVDS channel A differential signal pair 3
LVDS_A3-	115		
LVDS_A_CLK+	119	O	LVDS channel A differential clock pair
LVDS_A_CLK-	121		
LVDS_B0+	100	O	LVDS channel B differential signal pair 0
LVDS_B0-	102		
LVDS_B1+	104	O	LVDS channel B differential signal pair 1
LVDS_B1-	106		
LVDS_B2+	108	O	LVDS channel B differential signal pair 2
LVDS_B2-	110		
LVDS_B3+	114	O	LVDS channel B differential signal pair 3
LVDS_B3-	116		
LVDS_B_CLK+	120	O	LVDS channel B differential clock pair
LVDS_B_CLK-	122		
LVDS_PPEN	111	O	LVDS flat panel power enable
LVDS_BLEN	112	O	LVDS flat panel backlight enable
LVDS_BLT_CTRL	123	O	LVDS flat panel backlight brightness control via pulse width modulation.
LVDS_BLC_DAT/eDP0_HPD#	126	IO	Control data signal for external SSC clock chip
LVDS_BLC_CLK/eDP1_HPD#	128	IO	Control clock signal for external SSC clock chip
LVDS_DID_DAT/GP2_I2C_DAT	125	IO	General Purpose I^2C bus data line / DisplayID DDC data line used for LVDS flat panel detection
LVDS_DID_CLK/GP2_I2C_CLK	127	IO	General Purpose I^2C bus clock line / DisplayID DDC clock line used for LVDS flat panel detection

Table 20: LVDS signal definition

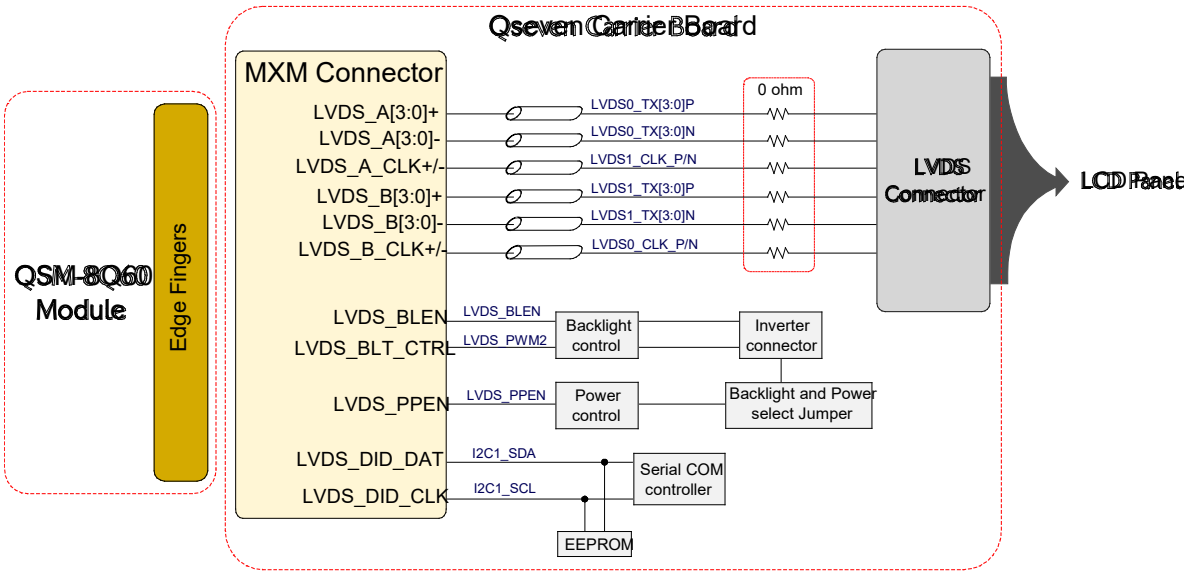

Figure 31: LVDS panel interface implementation

4.4.1. LVDS Layout and Routing Recommendations

The layout and routing recommendations for the LVDS interface in carrier board are listed below:

- Differential pairs should all be referenced to ground.
- Each trace of differential pairs should not have more than two via holes.
- Each differential pair signal (LVDS_A[3:0]±, LVDS_B[3:0]±) and clock differential pair (LVDS_A_CLK±, LVDS_B_CLK±) should be routed parallel to each other with the same trace length.
- Clock differential pair signals (LVDS_A_CLK±, LVDS_B_CLK±) should be length matched <20 mils.
- Route the LVDS pairs on a single layer adjacent to a ground plane.

Routing, layout, and trace properties for implementing LVDS interface in the carrier board are listed in the following tables.

Signal Group	Signal Name	Signal Reference	Topology	Signal Type
Data	LVDS_A[3:0]+	Ground or Power	Point to Point	Differential Data I/O Pairs
	LVDS_A[3:0]-			
	LVDS_B[3:0]+			
	LVDS_B[3:0]-			
Clock	LVDS_A_CLK+	Ground or Power	Point to Point	Differential Data I/O Pairs
	LVDS_A_CLK-			
	LVDS_B_CLK+			
	LVDS_B_CLK-			
Control	LVDS_PPEN	Ground or Power	Point to Point	Single-ended
	LVDS_BLEN			
	LVDS_BLT_CTRL			
	LVDS_BLC_DAT	Ground or Power	Point to Point	Single-ended
	LVDS_BLC_CLK			
	LVDS_DID_DAT	Ground or Power	Point to Point	Single-ended
	LVDS_DID_CLK			

Table 21: LVDS interface routing guidelines

Signal Group	Signal Name	Routing Layer	Accumulated Trace Length	Note
Data	LVDS_A[3:0]+	Top or Bottom	<1.8″	Route each pair of wires in parallel
	LVDS_A[3:0]-			
	LVDS_B[3:0]+			
	LVDS_B[3:0]-			
Clock	LVDS_A_CLK+	Top or Bottom	<1.8″	Route each pair of wires in parallel
	LVDS_A_CLK-			
	LVDS_B_CLK+			
	LVDS_B_CLK-			
Control	LVDS_PPEN	Top or Bottom	<1.8″	
	LVDS_BLEN			
	LVDS_BLT_CTRL			
	LVDS_BLC_DAT	Top or Bottom	<1.8″	
	LVDS_BLC_CLK			
	LVDS_DID_DAT	Top or Bottom	<1.8″	
	LVDS_DID_CLK			

Table 22: LVDS interface layout guidelines

Signal Name	Trace Impedance	Trace & Spacing (mil) (S : W : S1 : W : S)	Pair to Pair Length Mismatch	Spacing to Other Groups
LVDS_A[3:0]+	100Ω ± 15%	20 : 5 : 8 : 5 : 20	5 mils	20 mils
LVDS_A[3:0]-				
LVDS_B[3:0]+				
LVDS_B[3:0]-				
LVDS_A_CLK+	100Ω ± 15%	20 : 5 : 8 : 5 : 20	5 mils	20 mils
LVDS_A_CLK-				
LVDS_B_CLK+				
LVDS_B_CLK-				
LVDS_PPEN	55Ω	5 : 8	-	8 mils
LVDS_BLEN				
LVDS_BLT_CTRL				
LVDS_BLC_DAT	55Ω	5 : 8	-	8 mils
LVDS_BLC_CLK				
LVDS_DID_DAT	55Ω	5 : 8	-	8 mils
LVDS_DID_CLK				

Table 23: LVDS interface trace properties

4.4.2. LVDS Reference Schematics

The following reference circuitry is an example of how to implement the LVDS interface on the carrier board.

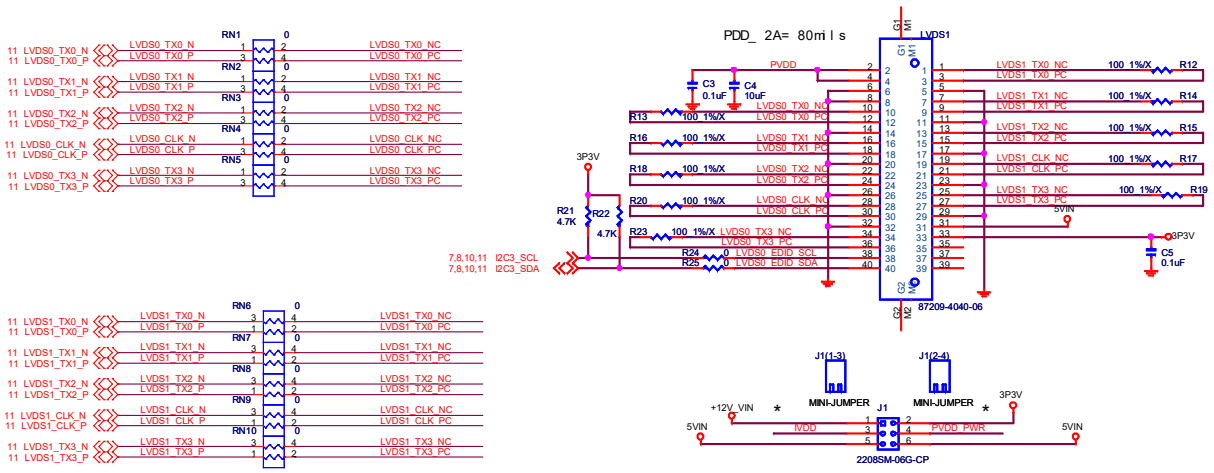

Figure 32: LVDS connector example

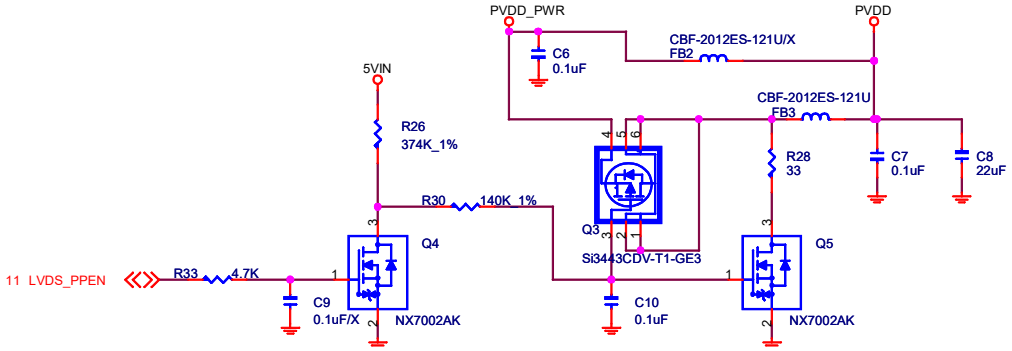

Figure 33: LVDS panel power reference circuitry

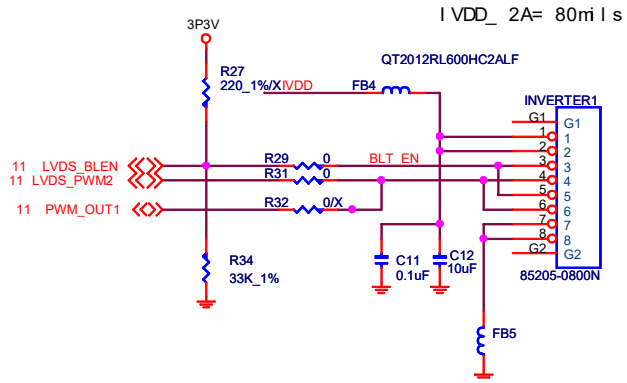

Figure 34: LVDS backlight reference circuitry

4.5. HDMI Interface

The VIA QSM-8Q60 supports one HDMI interface. The HDMI is used to connect high definition video and digital audio using a single cable. It allows connecting the digital video devices to utilize a high definition video signal.

HDMI interface uses four differential data pair signals that carries video and audio signals.

Signal Name	Shared with	Pin #	I/O	Description
TMDS_CLK+	DP_LANE3+	131	O	TMDS differential pair clock lines
TMDS_CLK-	DP_LANE3-	133		
TMDS_LANE0+	DP_LANE2+	143	O	TMDS differential pair lines lane 0
TMDS_LANE0-	DP_LANE2-	145		
TMDS_LANE1+	DP_LANE1+	137	O	TMDS differential pair lines lane 1
TMDS_LANE1-	DP_LANE1-	139		
TMDS_LANE2+	DP_LANE0+	149	O	TMDS differential pair lines lane 2
TMDS_LANE2-	DP_LANE0-	151		
HDMI_CTRL_DAT	-	150	IO	DDC based control signal (data) for HDMI device
HDMI_CTRL_CLK	-	152	IO	DDC based control signal (clock) for HDMI device
DP_HDMI_HPD#	-	153	I	Hot plug detection signal that serves as an interrupt request

Table 24: HDMI interface signal definition

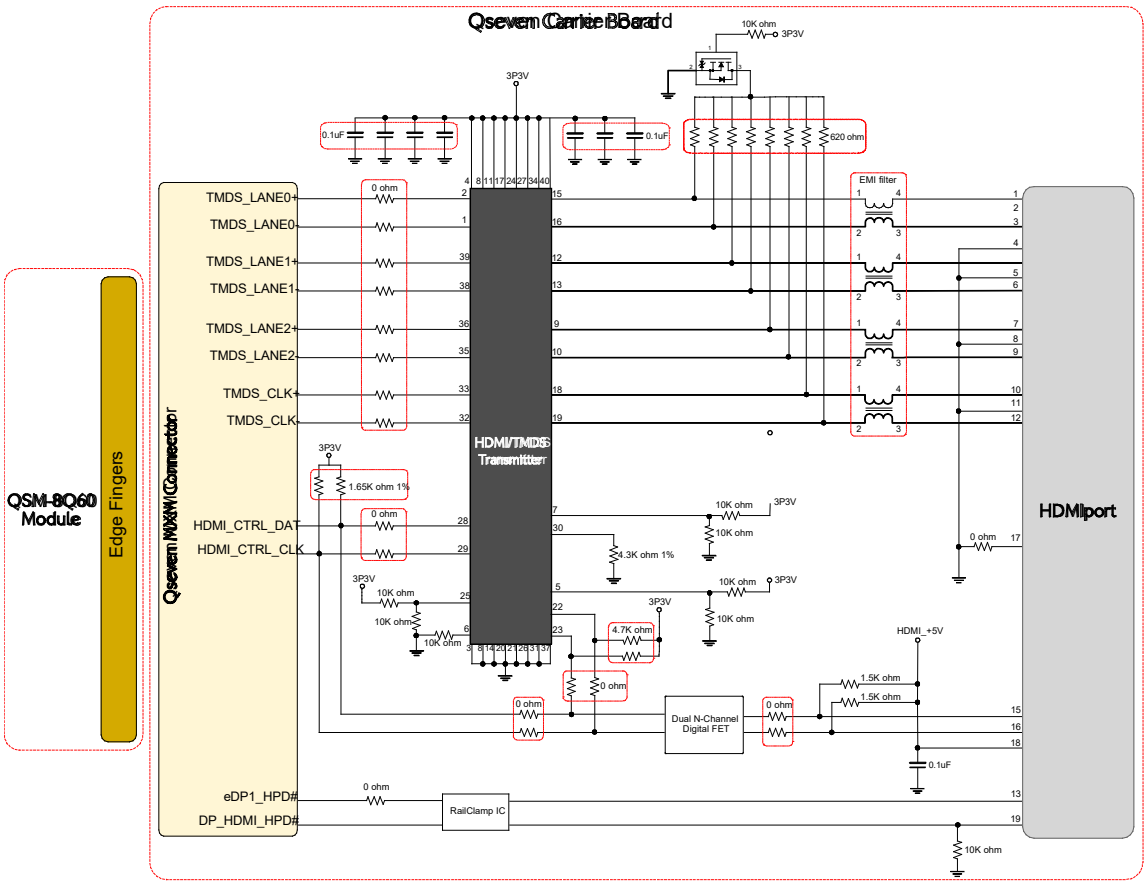

Figure 35: HDMI interface connector diagram

4.5.1. HDMI Layout and Routing Recommendations

- Differential pair should be all referenced to ground.
- Each trace of differential pairs should not have more than two via holes.
- Each differential pairs signal should route to parallel to each other with the same trace length.
- Route the differential pairs on a single layer adjacent to a ground plane.

Routing, layout and trace properties for implementing HDMI interface in the carrier board are listed in the following tables.

Signal Group	Signal Name	Signal Reference	Routing Topology	Signal Type
Data	TMDS_LANE0+	Ground	Point to Point	Differential Data I/O Pairs
	TMDS_LANE0-			
	TMDS_LANE1+			
	TMDS_LANE1-			
	TMDS_LANE2+			
	TMDS_LANE2-			
Clock	TMDS_CLK+	Ground	Point to Point	Differential Pairs
	TMDS_CLK-			
Control	HDMI_CTRL_DAT	Ground	Point to Point	Single-ended
	HDMI_CTRL_CLK			
	DP_HDMI_HPD#			

Table 25: HDMI interface routing guidelines

Signal Group	Signal Name	Routing Layer	Accumulated Trace Length	Note
Data	TMDS_LANE0+	Top or Bottom	< 3.3"	
	TMDS_LANE0-			
	TMDS_LANE1+			
	TMDS_LANE1-			
	TMDS_LANE2+			
	TMDS_LANE2-			
Clock	TMDS_CLK+	Top or Bottom	<3.3"	
	TMDS_CLK-			
Control	HDMI_CTRL_DAT	Top or Bottom		
	HDMI_CTRL_CLK			
	DP_HDMI_HPD#			

Table 26: HDMI interface layout guidelines

Signal Name	Trace Impedance	Trace & Spacing (mil) (S : W : S1 : W : S)	Spacing to Other Signal	Pair to Pair Length Mismatch
TMDS_LANE0+	100Ω ± 15%	15 : 5 : 6 : 5 : 15	15 mils	< 100 mils
TMDS_LANE0-				
TMDS_LANE1+				
TMDS_LANE1-				
TMDS_LANE2+				
TMDS_LANE2-				
TMDS_CLK+	100Ω ± 15%	5 : 6	15 mils	< 100 mils
TMDS_CLK-				
HDMI_CTRL_DAT	55Ω ± 15%	5 : 6	6 mils	-
HDMI_CTRL_CLK				
DP_HDMI_HPD#				

Table 27: HDMI interface trace properties

4.5.2. HDMI Reference Schematics

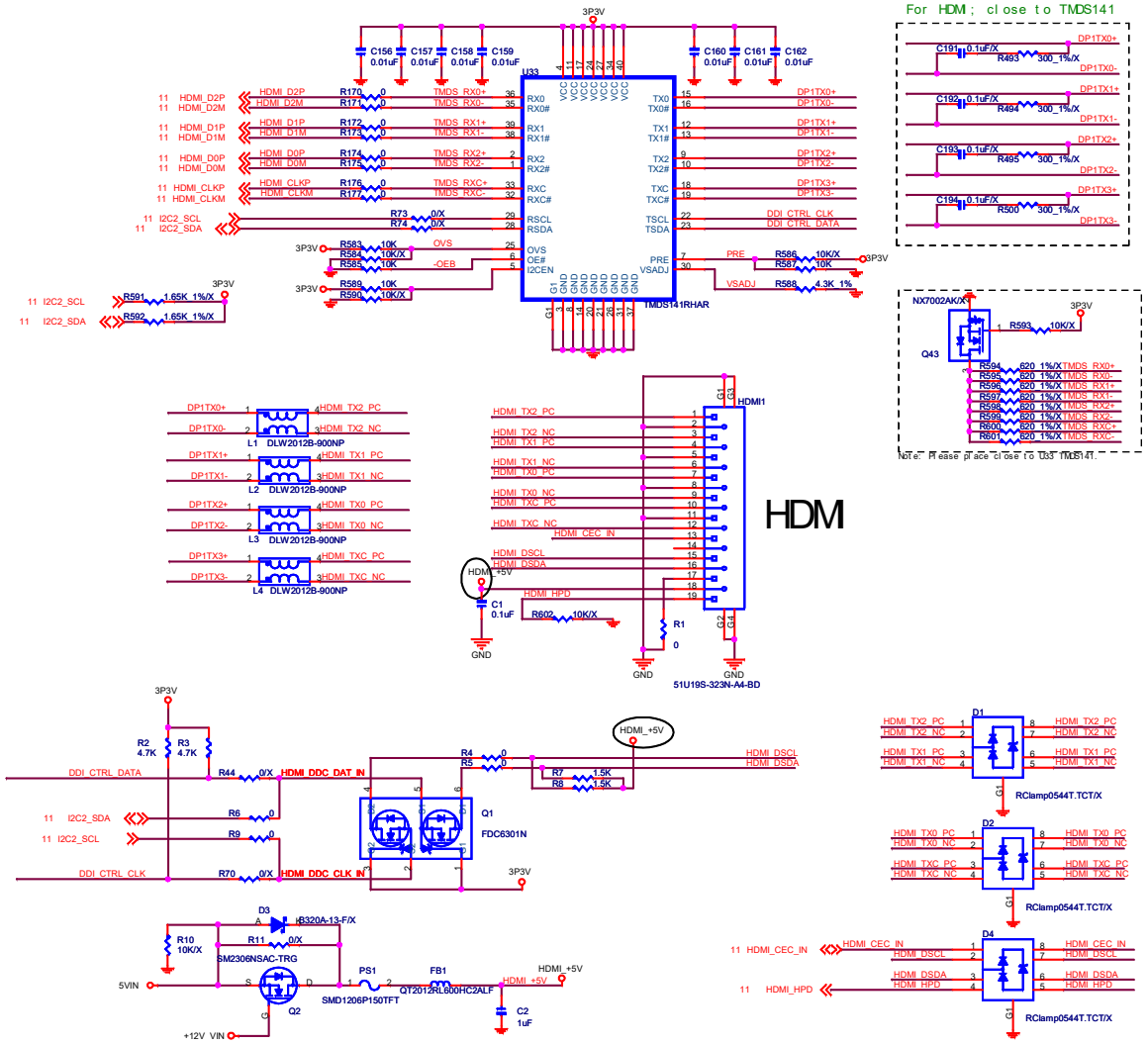

Figure 36: HDMI interface reference circuitry

4.6. Audio Interface

The Audio interface is a link between the VIA QSM-8Q60 module and Audio Codec that supports the I²S bus in the carrier board. This section contains I²S layout and routing information.

The corresponding audio interface signals are defined in the table below.

Signal Name	Pin #	I/O	Description
HDA_RST#/I2S_RST#	61	O	Codec reset
HDA_SYNC/I2S_WS	59	O	Serial Sample Rate Synchronization
HDA_BITCLK/I2S_CLK	63	O	Bit clock for Codec
HDA_SDO/I2S_SDO	67	O	Serial Data Output to Codec
HDA_SDI/I2S_SDI	65	I	Serial Data Input Stream from Codec

Table 28: Audio interface signal definition

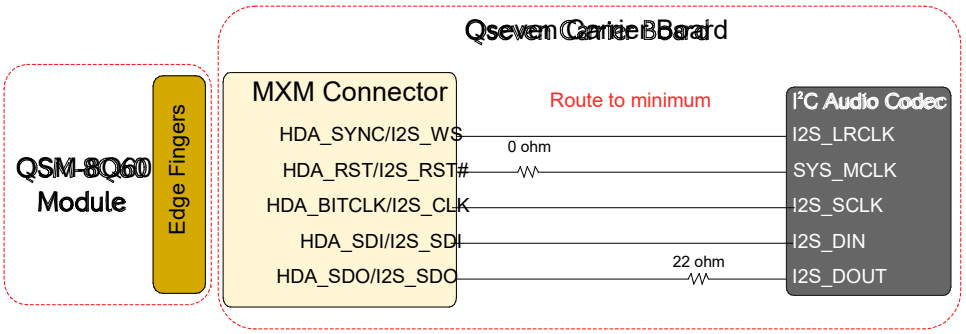

Figure 37: Onboard I²S audio codec implementation example

4.6.1. Audio Layout and Routing Recommendations

- Route the analog and digital trace signals as far as possible from each other to prevent noise.
- Route the clock trace away from any analog input and voltage reference pins.
- Isolate the codec or put away from any major current path or ground bounce.
- Fill with copper the regions between the analog traces and attached it to the analog ground.
- Fill with copper the regions between the digital traces and attached it to the digital ground.

Note:
For optimizing timing and signal quality issues, the values of the series resistors are design dependent and should be verified.

Routing, layout and trace properties for implementing audio interface in the carrier board are listed in the following tables.

Signal Name	Signal Reference	Topology	Signal Type
HDA_RST#/I2S_RST#	Ground or Power	Point to Point	Single-ended
HDA_SYNC/I2S_WS			
HDA_BITCLK/I2S_CLK	Ground or Power	Point to Point	Single-ended
HDA_SDO/I2S_SDO	Ground or Power	Point to Point	Single-ended
HDA_SDI/I2S_SDI	Ground or Power	Point to Point	Single-ended

Table 29: Audio interface routing guidelines

Signal Name	Routing Layer	Accumulated Trace Length	Note
HDA_RST#/I2S_RST#	Top or Bottom		Route traces as short as possible
HDA_SYNC/I2S_WS			
HDA_BITCLK/I2S_CLK	Top or Bottom		
HDA_SDO/I2S_SDO	Top or Bottom		
HDA_SDI/I2S_SDI			

Table 30: Audio interface layout guidelines

Signal Name	Trace Impedance	Trace Width and Spacing (mil)	Spacing to Other Signal
HDA_RST#/I2S_RST#	55Ω ± 10%	5 : 10	
HDA_SYNC/I2S_WS			
HDA_BITCLK/I2S_CLK	55Ω ± 10%	5 : 20	
HDA_SDO/I2S_SDO	55Ω ± 10%	5 : 10	
HDA_SDI/I2S_SDI			

Table 31: Audio interface trace properties

4.6.2. Audio Reference Schematics

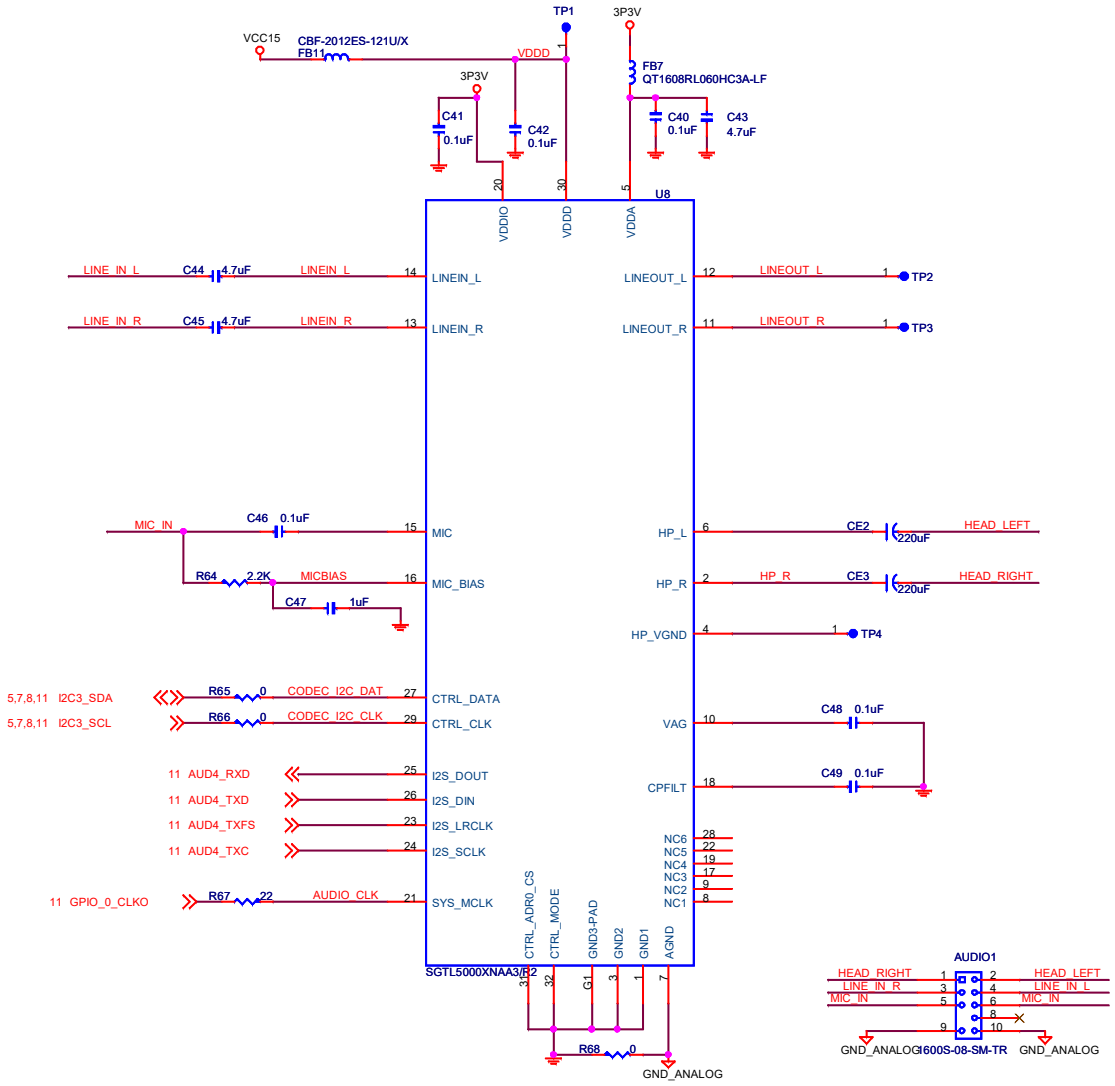

Figure 38: I²S Audio Codec implementation example

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