USER MANUAL

VIA EPIA-M920

Highly-integrated low-power platform with rich feature set and multimedia capabilities

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FCC-A Radio Frequency Interference Statement

This equipment has been tested and found to comply with the limits for a class A digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his personal expense.

Notice 1

The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Notice 2

Shielded interface cables and A.C. power cord, if any, must be used in order to comply with the emission limits.

Notice 3

The product described in this document is designed for general use, VIA Technologies assumes no responsibility for the conflicts or damages arising from incompatibility of the product. Check compatibility issue with your local sales representatives before placing an order.

Tested To Comply
With FCC Standards
FOR HOME OR OFFICE USE

Battery Recycling and Disposal

- ☐ Only use the appropriate battery specified for this product.
- ☐ Do not re-use, recharge, or reheat an old battery.
- ☐ Do not attempt to force open the battery.
- ☐ Do not discard used batteries with regular trash.
- ☐ Discard used batteries according to local regulations.

Safety Precautions

- ☐ Always read the safety instructions carefully.
- ☐ Keep this User's Manual for future reference.
- ☐ All cautions and warnings on the equipment should be noted.
- ☐ Keep this equipment away from humidity.
- ☐ Put this equipment on a reliable flat surface before setting it up.
- ☐ Check the voltage of the power source and adjust properly 110/220V before connecting the equipment to the power inlet.
- ☐ Do not place the power cord where people will step on it.
- ☐ Always unplug the power cord before inserting any add-on card or module.
- ☐ If any of the following situations arise, get the equipment checked by authorized service personnel:
  - The power cord or plug is damaged.
  - Liquid has entered into the equipment.
  - The equipment has been exposed to moisture.
  - The equipment is faulty or you cannot get it work according to User's Manual.
  - The equipment has been dropped and damaged.
  - The equipment has an obvious sign of breakage.
- ☐ Do not leave this equipment in extreme temperatures or in a storage temperature above 60°C (140°F). The equipment may be damaged.
- ☐ Do not leave this equipment in direct sunlight.
- ☐ Never pour any liquid into the opening. Liquid can cause damage or electrical shock.
- ☐ Do not place anything over the power cord.
- ☐ Do not cover the ventilation holes. The openings on the enclosure protect the equipment from overheating.

Box Contents

EPIA-M920-20Q SKU

☐ 1 x VIA EPIA-M920 board (with 2.0GHz VIA QuadCore E-Series)- with Fan
☐ 1 x SATA cable
☐ 1 x I/O bracket

EPIA-M920-16QE SKU

☐ 1 x VIA EPIA-M920 board (with 1.6GHz VIA Eden® X4) - Fanless
☐ 1 x SATA cable
☐ 1 x I/O bracket

Ordering Information

Model Name	Description
EPIA-M920-20Q	Mini-ITX board with 2.0GHz VIA QuadCore E-Series CPU with 2 HDMI, VGA, 2 LVDS, 3 USB 3.0, 6 USB 2.0, 4 COM, 2 Gigabit Ethernet, 2 SATA, PCIe x4 slot, ATX power connector
EPIA-M920-16QE	Mini-ITX board with 1.6GHz VIA Eden® X4 CPU with 2 HDMI, VGA, 2 LVDS, 3 USB 3.0, 6 USB 2.0, 4 COM, 2 Gigabit Ethernet, 2 SATA, PCIe x4 slot, ATX power connector

Optional Accessories

Wireless Modules

Part Number	Description
EMIO-1533-00A2	VNT9271 IEEE 802.11b/g/n USB Wi-Fi module with assembly kit and antenna
EMIO-5531-00A1	VAB-820-W IEEE 802.11b/g/n USB Wi-Fi & Bluetooth module with assembly kit and antenna

Table of Contents

List of Figures

List of Tables

1. Product Overview

The VIA EPIA-M920 is a high performance native x86 board designed mainly for embedded, POS, Kiosk, ATM and digital media application. It can also be used for various domain applications such as desktop PC, industrial PC, etc. The VIA EPIA-M920 is based on the VIA VX11H MSP (Media System Processor) chipset that features the VIA C-640 DX11 with 2D/3D graphics and video accelerators for rich digital media performance.

The VIA EPIA-M920 includes a powerful, secure, and efficient VIA QuadCore E-Series/VIA Eden® X4 processor. The VIA QuadCore E-Series/VIA Eden® X4 processor includes the VIA AES Security Engine, VIA CoolStream™ Architecture and VIA PowerSaver™ Technology.

The VIA EPIA-M920 has two 1333MHz DDR3 SODIMM slots that support up to 16GB memory size. The VIA EPIA-M920 provides support for high fidelity audio with its included VIA VT2021 High Definition Audio Codec. In addition it supports two SATA 3Gb/s storage devices.

The VIA EPIA-M920 is compatible with a full range of Mini-ITX chassis as well as FlexATX and MicroATX enclosures and power supplies. The VIA EPIA-M920 is fully compatible with Microsoft® and Linux operating systems.

1.1. Key Features and Benefits

1.1.1. VIA QuadCore E-Series/VIA Eden® X4

The VIA QuadCore E-Series/VIA Eden® X4 is a 64-bit superscalar x86 quad core processor combine on two dies. It is based on advanced 28 nanometer process technology packed into an ultra-compact NanoBGA2 package measuring 21mm x 21mm. The VIA QuadCore E-Series/VIA Eden® X4 processor delivers a superb performance on multi-tasking, multimedia playback, productivity and internet browsing in a low power budget.

Note:
For Windows 7 and Windows Server 2008 R2 users only:
If encounter the issue such as the operating system recognizing the VIA Dual-Core CPU as two processors instead of one processor with two cores. Download and install the hotfix released by Microsoft to address this issue. The downloadable hotfix is available at http://support.microsoft.com/kb/2502664

VIA QuadCore E-Series and VIA Eden® X4 processors are ideal for embedded system applications such as industrial PCs, test machines, measuring equipment, digital signage, medical PCs, monitoring systems, gaming machines, in-vehicle entertainment, etc.

1.1.2. VIA VX11H MSP

The VIA VX11H is the fourth generation, highly integrated Media System Processor which provides high quality digital video streaming and high definition video playback. It features the VIA C-640 DX11 2D/3D graphics and video processor, High Definition video decoder and supports DDR3 1333 controller and USB 3.0 interface.

The VIA VX11H offers superb-graphics performance, immersive visual experience, and supports DirectX 11.0 that allows realistic 3D rendering and increased visual acuity. It is also based on a highly sophisticated power efficient architecture that enables such rich integration into a compact package.

1.1.3. Modular Expansion Options

The VIA EPIA-M920 ensures long-term usability with its support for industry standard expansion options. Its support for legacy PCI expansion cards helps to smooth and reduce the costs of transitioning to newer expansion technologies. The VIA EPIA-M920 enables companies to slowly roll out upgrades as necessary instead of having to replace everything all at once. This ensures that companies using the VIA EPIA-M920 obtain the maximum benefits from its past investments in PCI expansion cards.

The VIA EPIA-M920 also includes a 4-Lane PCI Express 2.0 expansion slot that provides protection against obsolescence.

1.2. Product Specifications

Processor
- 2.0GHz VIA QuadCore E-Series processor (for EPIA-M920-20Q)-with Fan
- 1.6GHz VIA Eden® X4 processor (for EPIA-M920-16QE)-Fanless

Chipset
- VIA VX11H Media System Processor

BIOS
- AMI Aptio UEFI BIOS, 4MB Flash memory

System Memory
- 2 x DDR3 1333 SODIMM slots
- Supports up to 8GB memory per slot

Note:
The real memory size may show less than 16GB due to some capacity are used for BIOS or other functions.

Storage
- 2 x SATA connectors

Graphics
- Integrated C-640 DX11 3D/2D graphics with MPEG-2, WMV9, VC-1, H.264 decoding acceleration

LAN
- Realtek-RTL8111G Gigabit Ethernet controller (for EPIA-M920-20Q and EPIA-M920-16QE)

Audio
- VIA VT2021 High Definition Audio Codec

Super I/O
- Fintek F71869E

Expansion I/O
- 1 x PCIe x4 slot

Onboard I/O
- 2 x SATA connectors
- 2 x SATA DOM power selectors
- 2 x USB 2.0 pin headers for 4 ports
- 1 x USB 3.0 connector for 1 port
- 1 x Dual channel 18/24-bit LVDS panel connector (DVP, VT1636)
- 1 x Single channel 18/24-bit LVDS panel connector (VX11H internal)
- 2 x Backlight control connectors for inverter power and brightness control
- 3 x COM pin headers (2 from VX11H, powered with selectable 5V/12V)
- 1 x LPC pin header
- 1 x SMBus pin header
- 1 x S/PDIF-out connector
- 1 x Digital I/O pin headers (4GPI + 4 GPO)
- 1 x Front audio pin header (for Line-out and Mic-in)
- 2 x Smart Fan pin headers for CPU and System
- 1 x SD card (SDHC/SDXC) pin header
- 1 x ATX power connector

- 1 x PCIe x4 slot
- 1 x PS/2 keyboard and mouse pin header
- 1 x Front panel pin header
- 1 x External thermal resister pin header
- 1 x SPI pin header

Onboard Jumper

- 1 x Clear CMOS jumper
- 1 x SATA DOM jumper
- 1 x COM1 and COM2 voltage jumper
- 1 x COM3 and COM4 voltage jumper
- 1 x SPI address jumper
- 1 x VDD power jumper
- 1 x LVDS1 and LVDS2 power jumper
- 1 x DDR3 SODIMM voltage jumper

Back Panel I/O

- 2 x USB 3.0 ports
- 2 x USB 2.0 ports
- 2 x HDMI® ports
- 1 x VGA port
- 1 x COM port (powered with selectable 5V/12V)
- 2 x Gigabit Ethernet ports
- 3 x Audio jacks: Line-in, Line-out, and Mic-in
- 2 x PS/2 keyboard/mouse ports

Operating System

- Windows 10/8.1/8/7
- Windows Embedded Standard 7
- Windows Embedded POSReady 7
- Linux

Power Supply

- ATX power connector

System Monitoring & Management

- Wake-on-LAN, Keyboard Power-on, Timer Power-on, System power management, AC power failure recovery, Watchdog Timer

Operating Temperature

- 0°C ~ 60°C

Operating Humidity

- 0% ~ 95% (non-condensing)

Form Factor

- Mini-ITX
- 17cm x 17cm (6.7" x 6.7")

Compliance

- CE
- FCC

Note:
As the operating temperature provided in the specifications is a result of testing performed in a testing chamber, a number of variables can influence this result. Please note that the working temperature may vary depending on the actual situation and environment. It is highly recommended to execute a solid testing program and take all variables into consideration when building the system. Please ensure that the system is stable at the required operating temperature in terms of application.

1.3. Layout Diagram

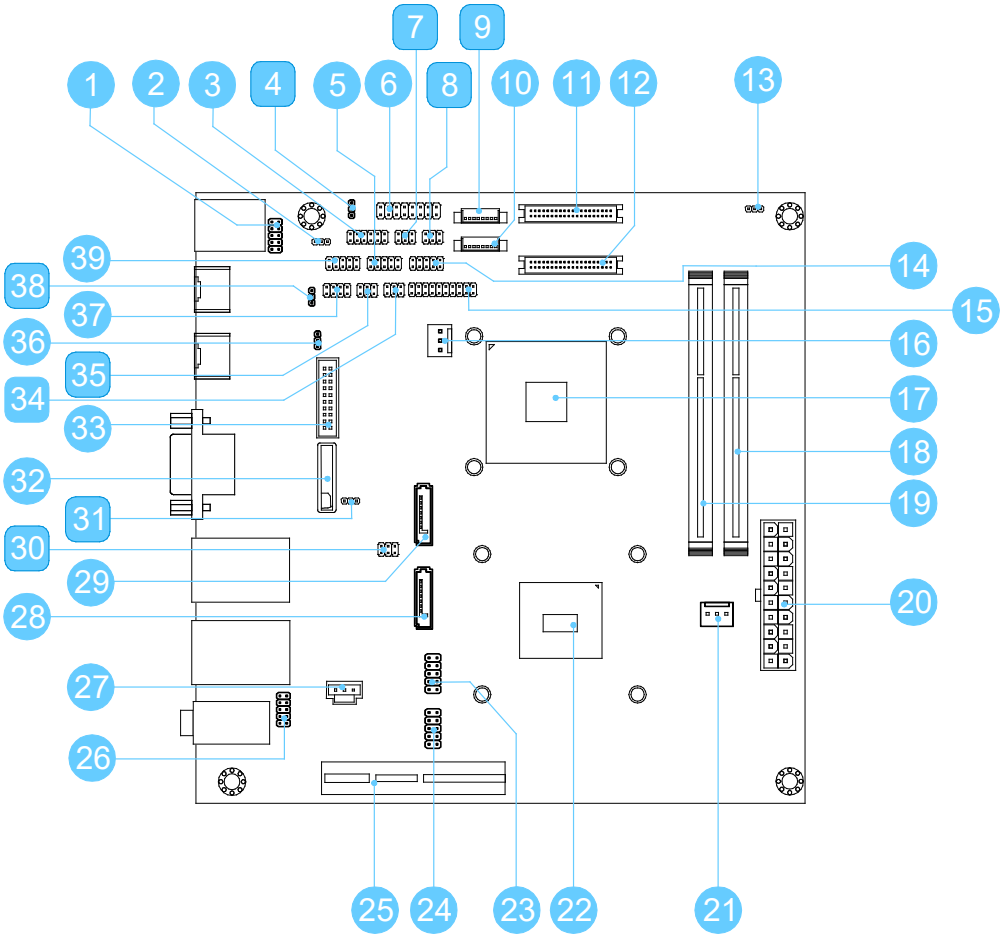

Figure 1: Layout diagram of the VIA EPIA-M920 (top side)

Item	Description
1	PS/2 keyboard and mouse pin header (JKBMS)
2	SMBus pin header (SMBUS1)
3	Digital I/O pin headers (DIO1)
4	VDD power jumper (J9)
5	COM4 pin header (COM4)
6	Front panel pin header (F_PANEL)
7	LVDS1 power jumper (J14)
8	LVDS2 power jumper (J15)
9	Backlight control connector 2 (INVERTER2)
10	Backlight control connector 1 (INVERTER1)
11	LVDS panel connector 2 (LVDS2)
12	LVDS panel connector 1 (LVDS1)
13	DDR3 SODIMM voltage jumper (J16)
14	COM3 pin header (COM3)
15	LPC pin header (LPC1)
16	System fan connector (SYSFAN)
17	VIA VX11H chipset
18	Memory slot 2 (SODIMM2)

19	Memory slot 1 (SODIMM1)
20	ATX power supply connector (ATX_POWER2)
21	CPU fan connector (CPUFAN)
22	VIA CPU
23	USB 2.0 pin header 1 (USB_1)
24	USB 2.0 pin header 2 (USB_2)
25	PCI Express x4 slot
26	Front audio pin header (F_AUDIO1)
27	S/PDIF connector (SPDIF1)
28	SATA connector 1 (SATA1)
29	SATA connector 2 (SATA2)
30	SATA DOM power jumper (J12)
31	Clear CMOS jumper (J10)
32	CMOS battery slot (BAT1)
33	USB 3.0 connector (J8)
34	COM3 and COM4 voltage jumper (J13)
35	COM1 and COM2 voltage jumper (J11)
36	External Thermal Resister pin header (J7)
37	SPI pin header (SPI1)
38	SPI address jumper (J6)
39	COM2 pin header (COM2)

Table 1: Layout diagram description table of the VIA EPIA-M920

1.4. Product Dimensions

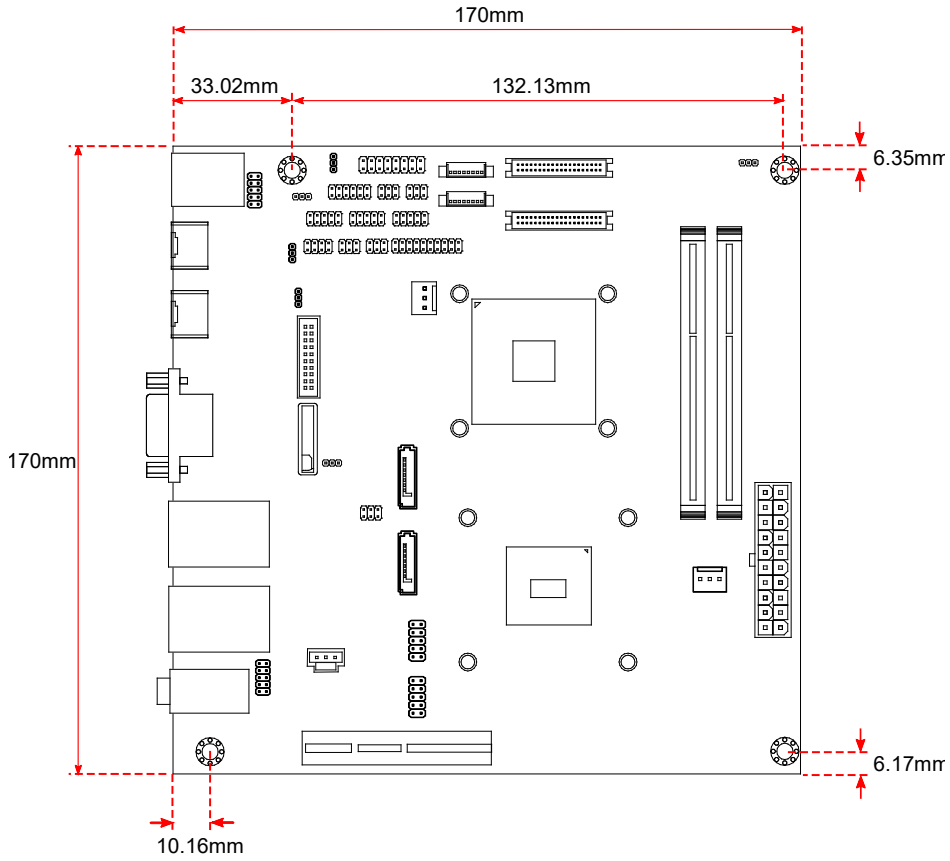

Figure 2: Mounting holes and dimensions of the VIA EPIA-M920

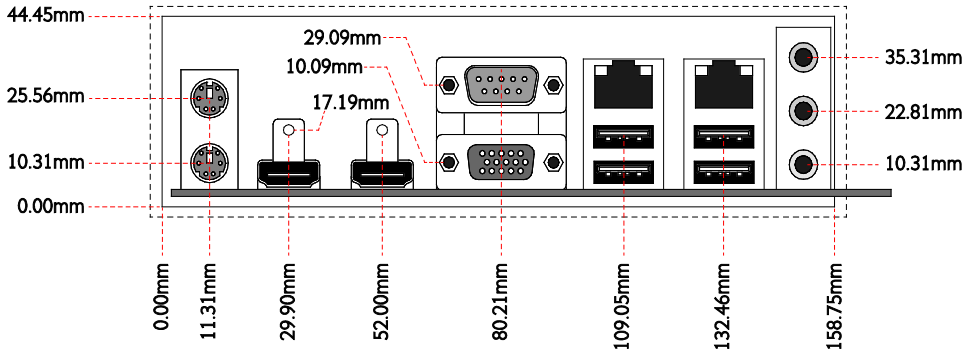

Figure 3: External I/O port dimensions of the VIA EPIA-M920

1.5. Height Distribution

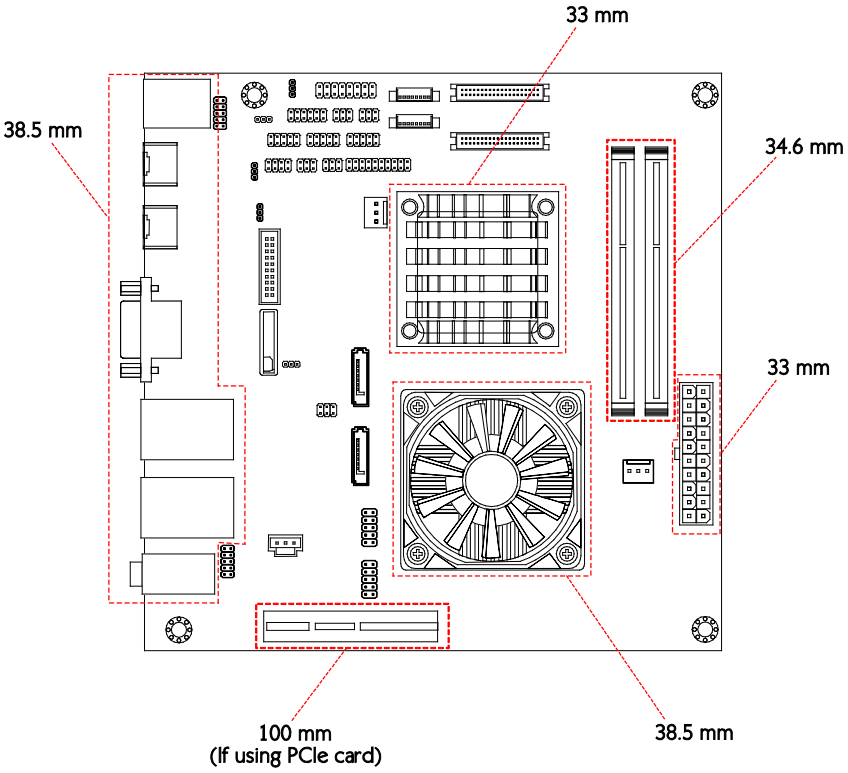

Figure 4: Height distribution of the VIA EPIA-M920 (for fan model)

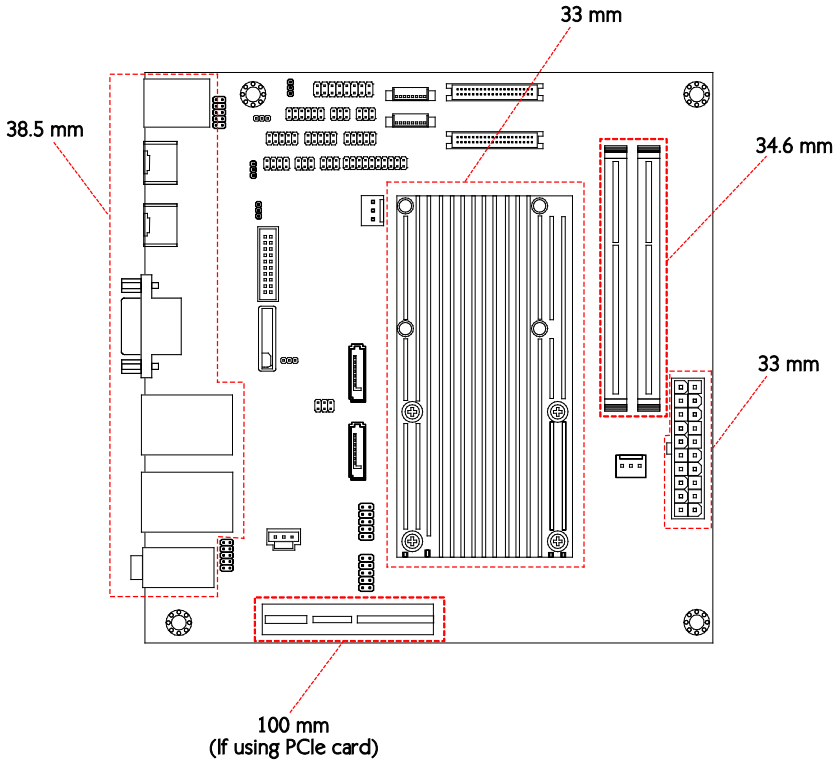

Figure 5: Height distribution of the VIA EPIA-M920 (for fanless model)

Note:
All other heights are under 21mm.

2. I/O Interface

The VIA EPIA-M920 has a wide selection of interfaces, and includes a selection of frequently used ports as part of the external I/O coastline.

2.1. External I/O Ports

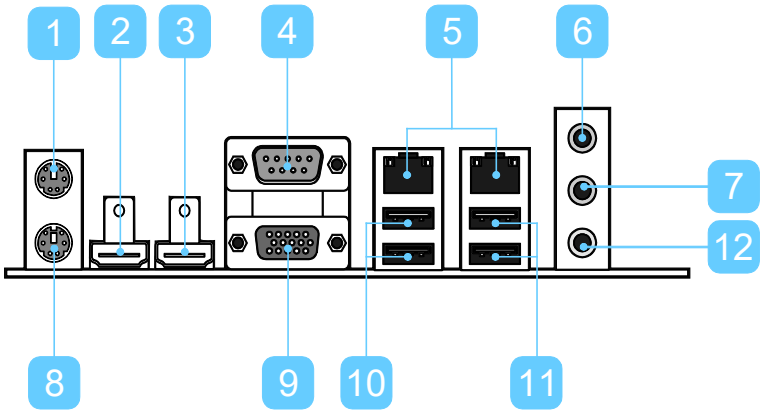

Figure 6: Back panel I/O ports

Item	Description
1	PS/2 mouse port
2	HDMI port 1
3	HDMI port 2
4	COM port
5	Gigabit Ethernet ports
6	Line-in
7	Line-out
8	PS/2 keyboard port
9	VGA port
10	USB 3.0 ports
11	USB 2.0 ports
12	Mic-in

Table 2: Layout diagram description table of the back panel I/O ports

2.1.1. PS/2 Port

The VIA EPIA-M920 has two integrated PS/2 ports for a keyboard and mouse. Each port is using the 6-pin Mini-DIN connector. The color purple is used for a PS/2 keyboard while the color green is used for a PS/2 mouse. The pinouts of the PS/2 ports are shown below.

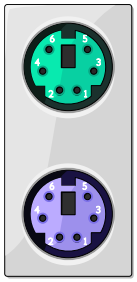

Figure 7: PS/2 port diagram

Pin	Signal
1	Data
2	NC
3	GND
4	+5V
5	Clock
6	NC

Table 3: PS/2 port pinouts

2.1.2. HDMI® Port

The integrated 19-pin HDMI® port uses an HDMI® Type A receptacle connector as defined in the HDMI® specification. The HDMI® (High Definition Multimedia Interface) port is for connecting the High Definition video and digital audio. The pinouts of the HDMI® port are shown below.

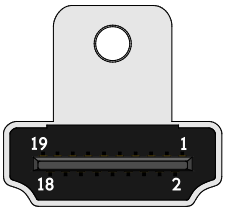

Figure 8: HDMI® port diagram

Pin	Signal	Pin	Signal
1	TX2+	2	GND
3	TX2-	4	TX1+
5	GND	6	TX1-
7	TX0+	8	GND
9	TX0-	10	TXC+
11	GND	12	TXC-
13	key	14	key
15	DDCSCL	16	DDCSDA
17	GND	18	+5V
19	Hot Plug Detect		

Table 4: HDMI® port pinouts

2.1.3. COM Port

The integrated 9-pin COM port uses a male DE-9 connector. The COM (COM1) port supports the RS-232 standard. The pinouts of the COM port are shown below.

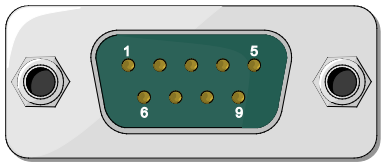

Figure 9: COM port diagram

Pin	Signal	Pin	Signal
1	DCD	6	DSR
2	RxD	7	RTS
3	TxD	8	CTS
4	DTR	9	RI
5	GND		

Table 5: COM port pinouts

2.1.4. Gigabit Ethernet Port

The integrated 8-pin Gigabit Ethernet port is using an 8 Position 8 Contact (8P8C) receptacle connector commonly known as RJ-45. The pinouts of the Gigabit Ethernet port are shown below.

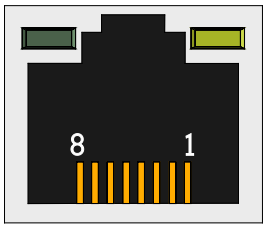

Figure 10: Gigabit Ethernet port diagram

Pin	Signal
1	Signal pair 1+
2	Signal pair 1-
3	Signal pair 2+
4	Signal pair 3+
5	Signal pair 3-
6	Signal pair 2-
7	Signal pair 4+
8	Signal pair 4-

Table 6: Gigabit Ethernet port pinouts

Each Gigabit Ethernet port has two individual LED indicators located on the front side to show its Active/Link status and Speed status.

	Active LED (Left LED on RJ-45 connector)	Link LED (Right LED on RJ-45 connector)
Link Off	Off	Off
Speed_10Mbit	Flash in Green color	Off
Speed_100Mbit	Flash in Green color	The LED is always On in Green color
Speed_1000Mbit	Flash in Green color	The LED is always On in Orange color

Table 7: Gigabit Ethernet port LED color definition

2.1.5. Audio Jack

There are three audio jack receptacles integrated into a single stack on the I/O coastline. Each receptacle can fit a 3.5mm Tip Ring Sleeve (TRS) connector to enable connections to Line-in, Line-out, and Mic-in.

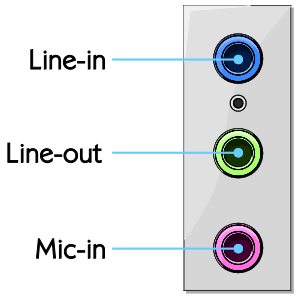

Figure 11: Audio jack receptacle stack

Wiring	Line-in	Line-out	Mic-in
Tip	Left channel in	Left channel	Left channel
Ring	Right channel in	Right channel	Right channel
Sleeve	Ground	Ground	Ground

Table 8: Audio jack receptacle pinouts

2.1.6. VGA Port

The integrated 15-pin VGA port uses a female DE-15 connector. The VGA port is for connecting to analog displays. The pinouts of the VGA port are shown below.

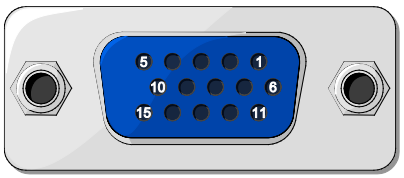

Figure 12: VGA port diagram

Pin	Signal
1	Red
2	Green
3	Blue
4	NC
5	GND
6	GND
7	GND
8	GND
9	+5V
10	NC
11	NC
12	SDA
13	HSync
14	VSync
15	SCL

Table 9: VGA port pinouts

2.1.7. USB 3.0 Port

The VIA EPIA-M920 is equipped with two USB 3.0 ports. Each USB 3.0 port has a maximum data transfer rate of up to 5Gb/s and is backwards compatible with the USB 2.0 specification. The USB 3.0 ports provides complete Plug and Play and hot swap capabilities for external devices. The pinouts of the USB 3.0 port are shown below.

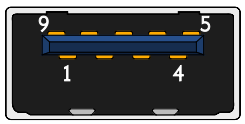

Figure 13: USB 3.0 port diagram

Pin	Signal
1	+5V
2	Data-
3	Data+
4	GND
5	Rx-
6	Rx+
7	GND
8	Tx-
9	Tx+

Table 10: USB 3.0 port pinout

2.1.8. USB 2.0 Port

The VIA EPIA-M920 is equipped with two USB 2.0 ports which gives complete Plug and Play and hot swap capability for external devices. The USB 2.0 interface complies with USB UHCI, Rev. 2.0. The pinouts of the USB 2.0 port are shown below.

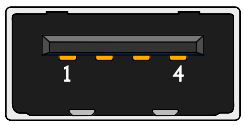

Figure 14: USB 2.0 port diagram

Pin	Signal
1	+5VSUS
2	Data-
3	Data+
4	GND

Table 11: USB 2.0 port pinouts

2.2. Onboard I/O

2.2.1. ATX Power Connector

The VIA EPIA-M920 has a 20-pin ATX power connector. The ATX power connector is labeled as "ATX_POWER1". The pinouts of the ATX power connector are shown below.

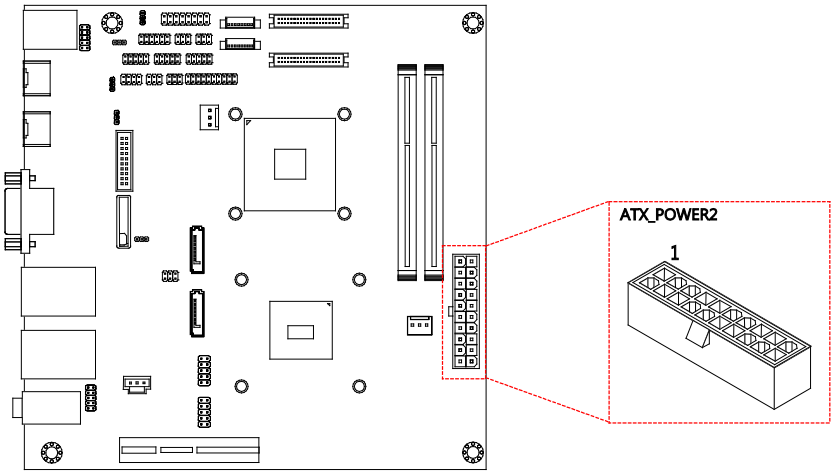

Figure 15: ATX power connector diagram

Pin	Signal	Pin	Signal
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	GND	13	GND
4	+5V	14	PS_ON
5	GND	15	GND
6	+5V	16	GND
7	GND	17	GND
8	PW-OK	18	-5V
9	+5VSUS	19	+5V
10	+12V	20	+5V

Table 12: ATX power connector pinouts

2.2.2. LVDS Panel Connector

The VIA EPIA-M920 has two LVDS panel connectors: LVDS1 and LVDS2. The LVDS1 panel connector is controlled by VIA VX11H chipset while the LVDS2 panel connector is controlled by VT1636 LVDS transmitter. The pinouts of the LVDS panel connectors are shown below.

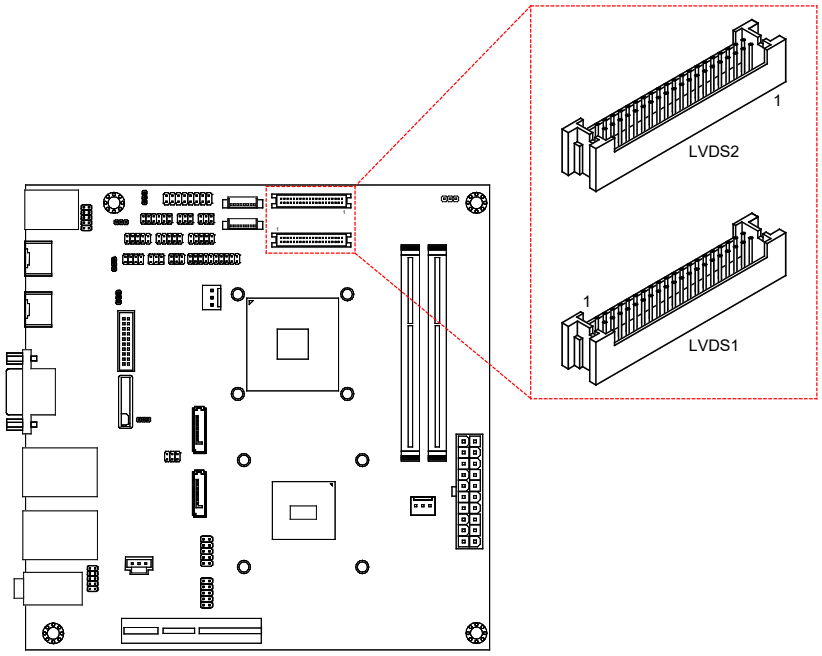

Figure 16: LVDS panel connector diagram

LVDS1			
Pin	Signal	Pin	Signal
M1	GND		
2	PVDD1	1	NC
4	PVDD1	3	NC
6	GND	5	GND
8	GND	7	NC
10	-LD1C0	9	NC
12	+LD1C0	11	GND
14	GND	13	NC
16	-LD1C1	15	NC
18	+LD1C1	17	GND
20	GND	19	NC
22	-LD1C2	21	NC
24	+ LD1C2	23	GND
26	GND	25	NC
28	-LCLK1	27	NC
30	+ LCLK1	29	NC
32	GND	31	GND
34	-LD1C3	33	NC
36	+ LD1C3	35	NC
38	LVDSPCLK	37	NC
40	LPDSPD	39	NC

LVDS2			
Pin	Signal	Pin	Signal
M1	GND		
2	PVDD2	1	-A4_L
4	PVDD2	3	A4_L
6	GND	5	GND
8	GND	7	-A5_L
10	-A0_L	9	A5_L
12	A0_L	11	GND
14	GND	13	-A6_L
16	-A1_L	15	A6_L
18	A1_L	17	GND
20	GND	19	-CLK2_L
22	-A2_L	21	CLK2_L
24	A2_L	23	GND
26	GND	25	-A7_L
28	-CLK1_L	27	A7_L
30	CLK1_L	29	NC
32	GND	31	NC
34	-A3_L	33	NC
36	A3_L	35	NC
38	DVPSPCLK	37	NC
40	DVPSPD	39	NC

Table 13: LVDS panel connectors pinouts

2.2.3. Backlight Control Connector

The VIA EPIA-M920 has two backlight control connectors labeled as INVERTER1 and INVERTER2. The backlight control connectors are for inverter power and brightness control. INVERTER1 corresponds to the LVDS1 panel connector. INVERTER2 corresponds to the LVDS2 panel connector. The pinouts of the backlight control connectors are shown below.

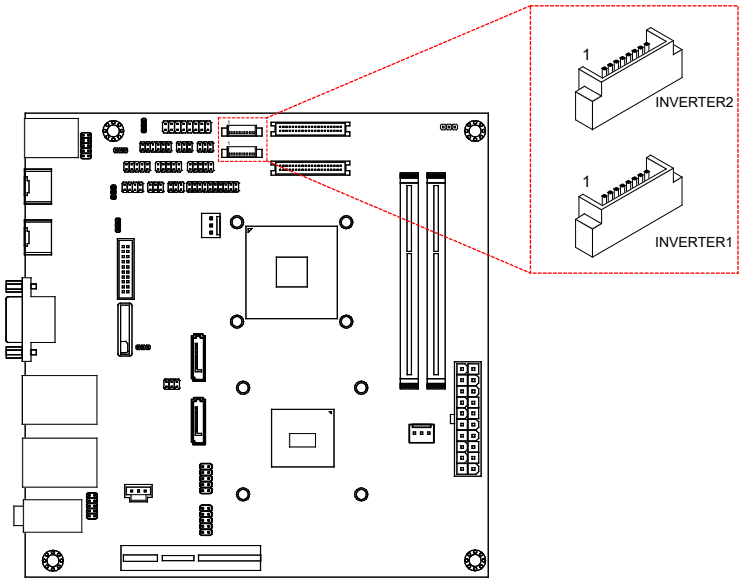

Figure 17: Backlight control connector diagram

INVERTER1	
Pin	Signal
1	INV1_12
2	INV1_12
3	BLON1
4	VX11PWM_CTL1
5	BLON1
6	BRIGHTNESS1_CTL1
7	GND
8	GND

INVERTER2	
Pin	Signal
1	IVDD2
2	IVDD2
3	BAKLITE
4	VX11PWM_CTL2
5	BAKLITE
6	BRIGHTNESS2_CTL2
7	GND
8	GND

Table 14: Backlight control connectors pinouts

2.2.4. Digital I/O Pin Header

The VIA EPIA-M920 includes one Digital I/O pin header that supports four GPO and four GPI pins. The pinouts of the Digital I/O pin header are shown below.

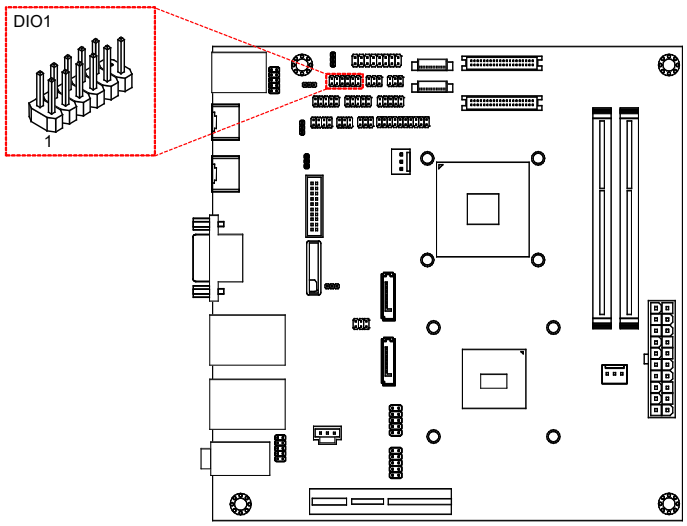

Figure 18: Digital I/O pin header diagram

Pin	Signal	Pin	Signal
1	5V_DIO	2	12V_DIO
3	GPO_37	4	GPI_53
5	GPO_36	6	GPI_52
7	GPO_35	8	GPI_51
9	GPO_34	10	GPI_50
11	GND		

Table 15: Digital I/O pin header pinouts

2.2.5. External Thermal Resister Pin Header

The VIA EPIA-M920 supports a pin header (3-pin) that allows the connection of a temperature sensor cable for detecting the system's internal air temperature. The temperature reading can be seen in the BIOS Setup Utility. The pin header is labeled as "J7". The pinouts of the external thermal resister pin header are shown below.

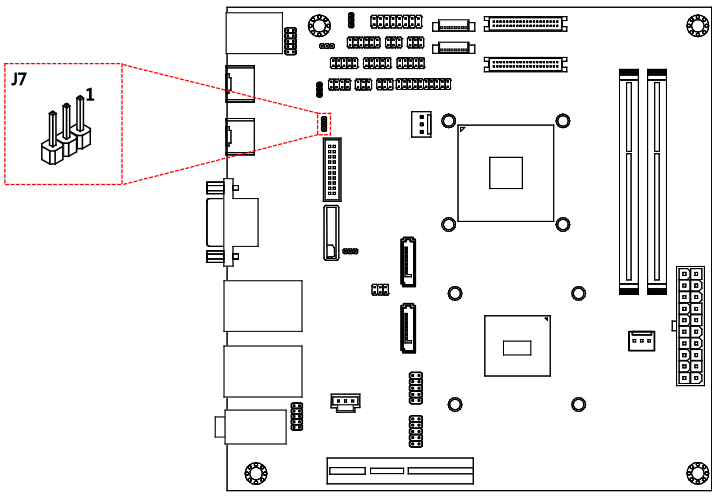

Figure 19: External thermal resister pin header diagram

Pin	Signal
1	TMPIN2
2	TMPIN2
3	HWMGND

Table 16: External thermal resister pin header pinouts

2.2.6. Front Panel Pin Header

The Front panel pin header consists of 15 pins in a 16-pin block. Pin 15 is keyed. The front panel pin header is labeled as "F_PANEL1". It provides access to system LEDs, power, reset, system speaker and HDD LED. The pinouts of the front panel pin header are shown below.

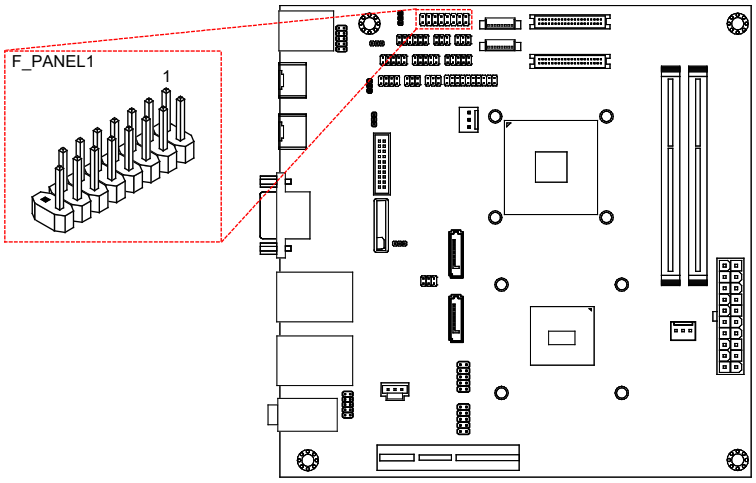

Figure 20: Front panel pin header diagram

Pin	Signal	Pin	Signal
1	+5VDUAL	2	+3.3V
3	+5VDUAL	4	SATA_LED
5	PWR_LED	6	PWR_BTN
7	+5V	8	GND
9	NC	10	-RST_SW
11	NC	12	GND
13	SPEAK	14	+5V
15	—	16	-SLEEPLED

Table 17: Front panel pin header pinouts

2.2.7. SMBus Pin Header

The SMBus pin header consists of 3 pins that allow connecting the SMBus devices. The devices communicate with an SMBus host and/or other SMBus devices using the SMBus interface. It is labeled as "SMBUS". The pinouts of the SMBus pin header are shown below.

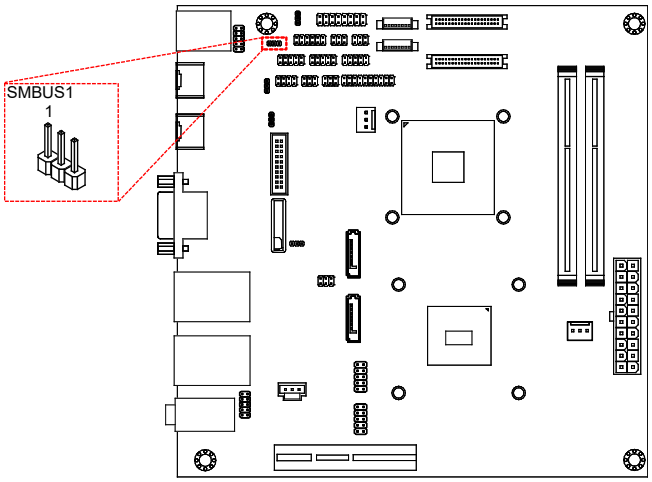

Figure 21: SMBus pin header diagram

Pin	Signal
1	SMBCK
2	SMBDT
3	GND

Table 18: SMBus pin header pinouts

2.2.8. CPU and System Fan Connectors

There are two fan connectors on board: one for the CPU and one for the chassis. The fan connector for the CPU is labeled as "CPUFAN1", and the fan connector for the system is labeled as "SYSFAN1". The fans provide variable fan speeds controlled by the BIOS. The pinouts of the fan connectors are shown below.

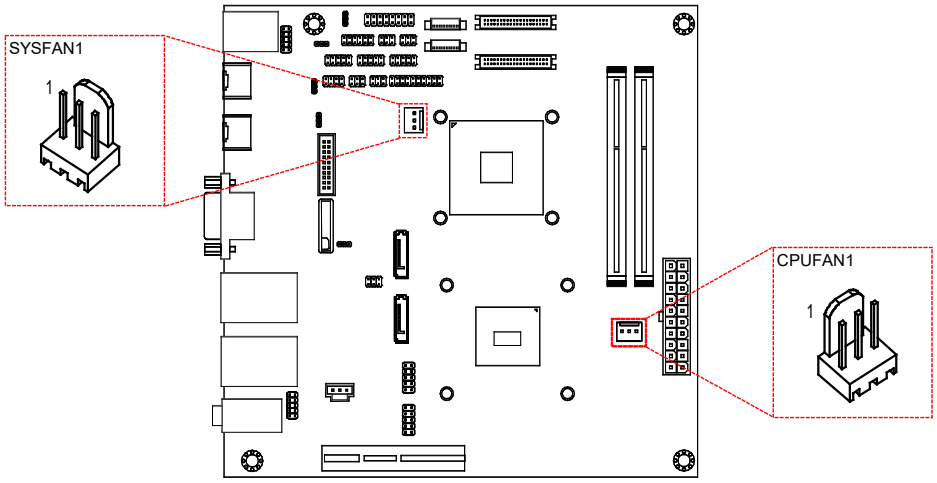

Figure 22: CPU and System fan connector diagram

CPUFAN1	
Pin	Signal
1	F_I01
2	F_PWM1
3	GND

SYSFAN1	
Pin	Signal
1	F_I02
2	F_PWM2
3	GND

Table 19: CPU and System fan connectors pinouts

2.2.9. SATA Connector

The two SATA connectors on board can support up to 3Gb/s transfer speeds. The SATA connectors are labeled as "SATA1" and "SATA2". The pinouts of the SATA connectors are shown below.

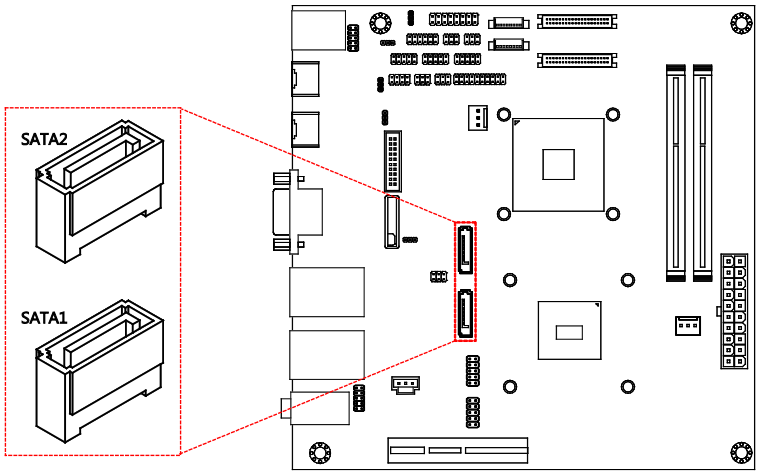

Figure 23: SATA connector diagram

SATA1	
Pin	Signal
1	GND
2	STXP_0
3	STXN_0
4	GND
5	SRXN_0
6	SRXP_0
7	SATA1_+5V

SATA2	
Pin	Signal
1	GND
2	STXP_1
3	STXN_1
4	GND
5	SRXN_1
6	SRXP_1
7	SATA2_+5V

Table 20: SATA connectors pinouts

Note:
If users want to use the SATA Disk-on-Module flash drive on the board, please use the SATA2 connector.

2.2.10. USB 2.0 Pin Header

The VIA EPIA-M920 has two USB 2.0 pin header blocks that support up to four USB 2.0 ports. The pin header blocks are labeled as "USB_1"and "USB_2. The pinouts of the USB 2.0 pin headers are shown below.

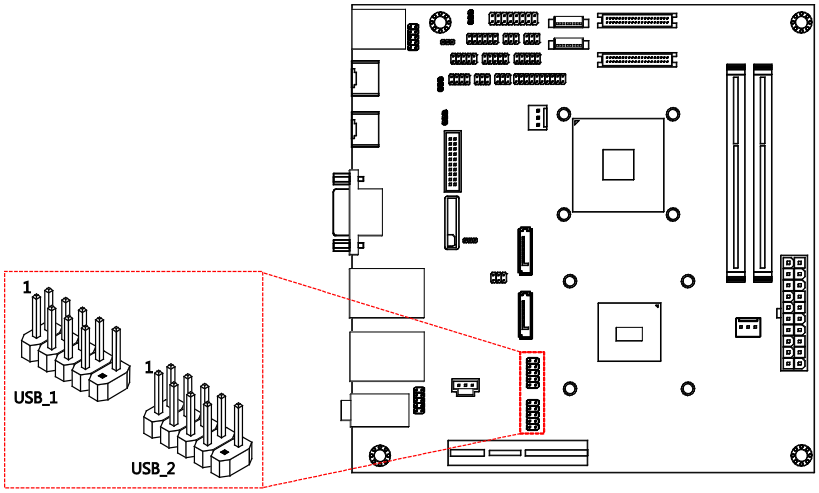

Figure 24: USB 2.0 pin header diagram

USB_1			
Pin	Signal	Pin	Signal
1	+5CDUAL	2	+5CDUAL
3	USBD_T1-	4	USBD_T0-
5	USBD_T1+	6	USBD_T0+
7	GND	8	GND
9	—	10	GND

USB_2			
Pin	Signal	Pin	Signal
1	+5CDUAL	2	+5CDUAL
3	USBD_T3-	4	USBD_T2-
5	USBD_T3+	6	USBD_T2+
7	GND	8	GND
9	—	10	GND

Table 21: USB 2.0 pin headers pinouts

2.2.11. COM Pin Header

There are a total of three COM pin headers on the VIA EPIA-M920. Each COM pin header supports the RS-232 standard. The pin headers are labeled as "COM2", "COM3", and "COM4". All of the COM pin headers can support +5V or +12V. The pinouts of the COM pin headers are shown below.

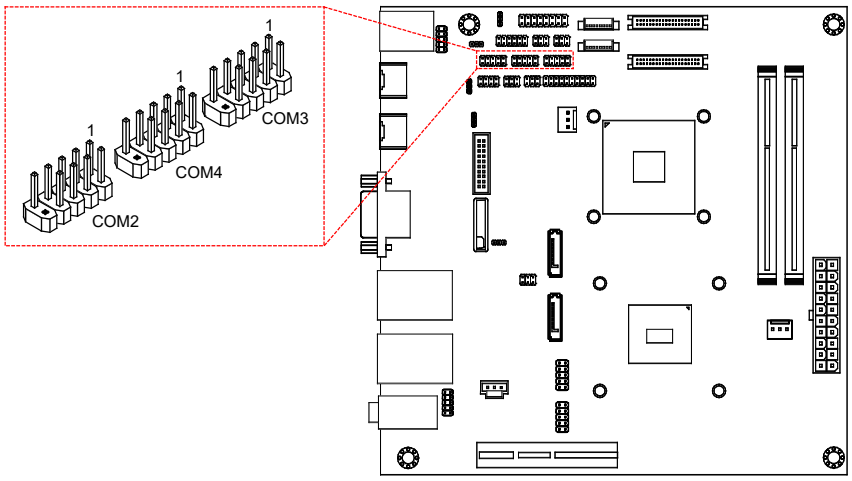

Figure 25: COM pin header diagram

Pin	Signal	Pin	Signal
1	COM_DCD	2	COM_RXD
3	GND	4	COM_DTR
5	GND	6	COM_DSR
7	COM_RTS	8	COM_CTS
9	COM_RI	10	—

Table 22: COM pin header pinouts

2.2.12. PS/2 Keyboard and Mouse Pin Header

The VIA EPIA-M920 has a pin header for a PS/2 keyboard and mouse. The pin header is labeled as "JKBMS". The pinouts of the PS/2 keyboard and mouse pin header are shown below.

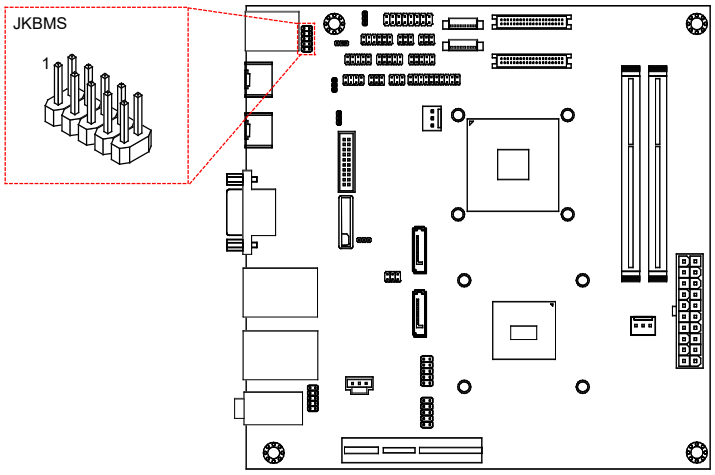

Figure 26: PS/2 keyboard and mouse pin header diagram

Pin	Signal	Pin	Signal
1	VCCE	2	GND
3	KBCK	4	KBDT
5	EKBCLK	6	EKBDATA
7	MSCK	8	MSDT
9	EMSCLK	10	EMSDATA

Table 23: PS/2 keyboard and mouse pin header pinouts

Note:
When the pin header is not in use, please short pin 3&5, pin 4&6, pin 7&9 and pin 8&10.

2.2.13. Front Audio Pin Header

In addition to the TRS audio jacks on the external I/O coastline, the VIA EPIA-M920 has a pin header for Line-out and Mic-in. The pin header is labeled as "F_AUDIO1". The pinouts of the front audio pin header are shown below.

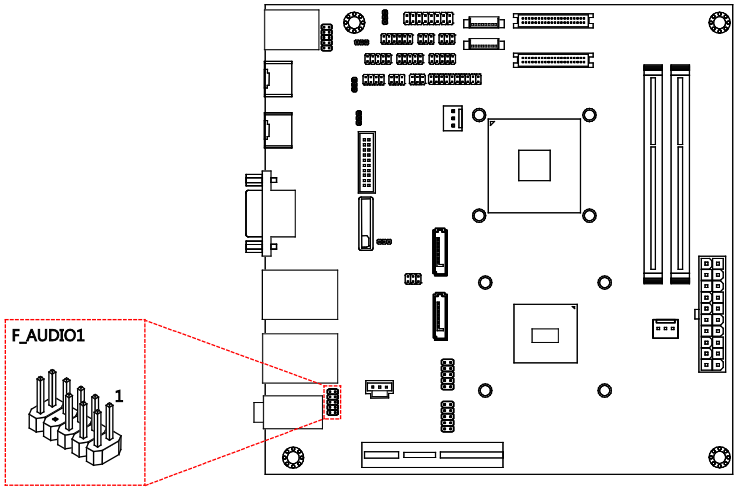

Figure 27: Front audio pin header

Pin	Signal	Pin	Signal
1	MIC2IN_L	2	AGND
3	MIC2IN_R	4	AGND
5	HPOUTR	6	MIC2_JD
7	F_AUDIO_SENSE	8	—
9	HPOUTL	10	HPOUT_JD

Table 24: Front audio pin header pinouts

2.2.14. SPI Pin Header

The VIA EPIA-M920 has one 8-pin SPI pin header. The SPI pin header is used to connect to the SPI BIOS programming fixture. The pin header is labeled as "SPI1". The pinouts of the SPI pin header are shown below.

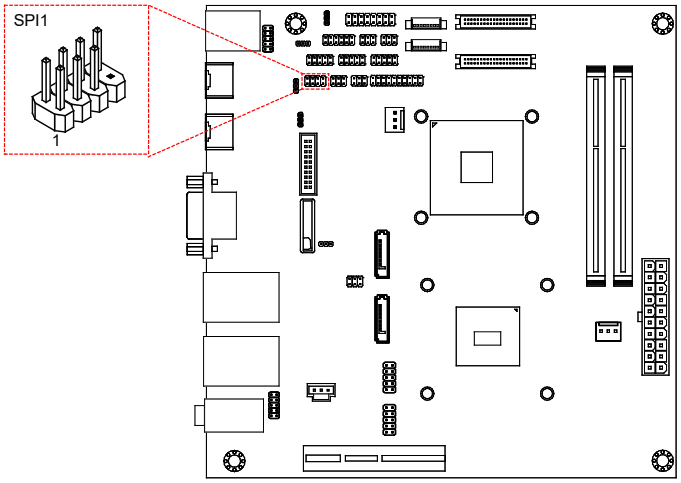

Figure 28: SPI pin header diagram

Pin	Signal	Pin	Signal
1	SPIVCC	2	GND
3	MSPISA	4	MSPICLK
5	MSPIDI	6	MSPIDO
7	—	8	-PCIRST

Table 25: SPI pin header pinouts

2.2.15. LPC Pin Header

The VIA EPIA-M920 has one LPC pin header for connecting LPC devices. The pin header is labeled as "LPC". The pinouts of the LPC pin header are shown below.

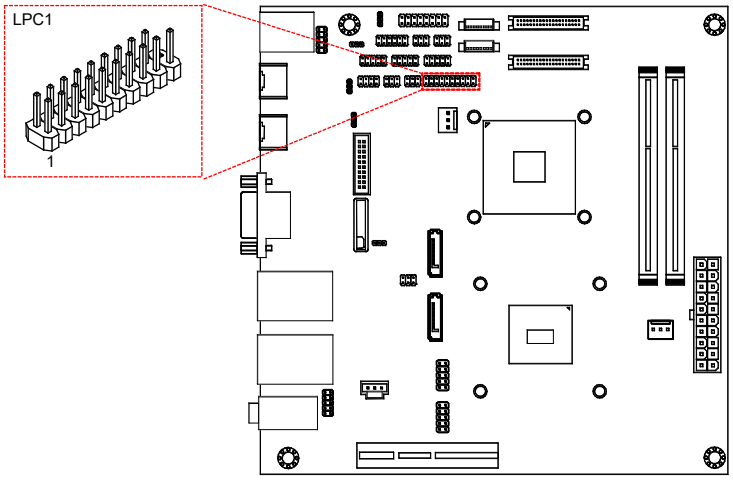

Figure 29: LPC pin header diagram

Pin	Signal	Pin	Signal
1	LPCAD1	2	LPC33CLK
3	-LPCRST	4	GND
5	LPCAD0	6	LPC48CLK
7	LPCAD2	8	-LPCFRAME
9	SERIRQ	10	LPCAD3
11	-LPCDRQ1	12	-EXTSMI
13	+5V	14	+3.3V
15	+5V	16	+3.3V
17	GND	18	GND
19	GND		

Table 26: LPC pin header pinouts

2.2.16. S/PDIF Connector

The VIA EPIA-M920 has one 3-pin S/PDIF (Sony Philips Digital Interface) connector. The S/PDIF output provides digital audio to external speakers or compressed AC3 data to an external Dolby Digital Decoder. The connector is labeled as "SPDIF". The pinouts of the S/PDIF connector are shown below.

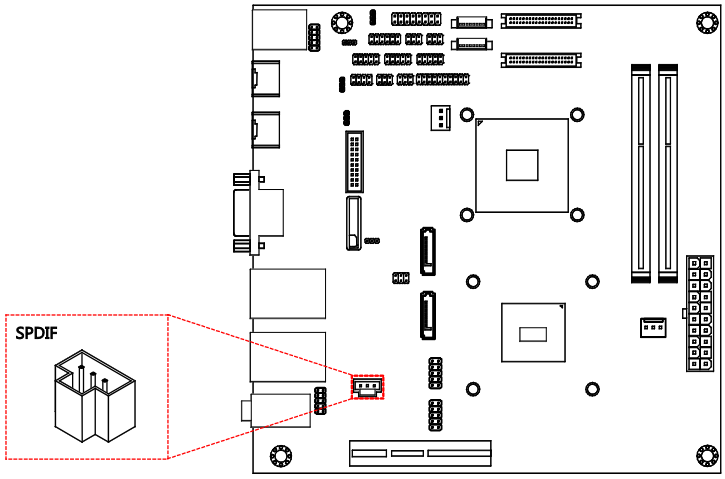

Figure 30: S/PDIF connector diagram

Pin	Signal
1	+5V
2	SPDIFO
3	GND

Table 27: S/PDIF connector pinouts

2.2.17. CMOS Battery Slot

The VIA EPIA-M920 is equipped with a CMOS battery slot, which is compatible with CR2032 coin batteries. The CMOS battery slot is labeled as "BAT2". When inserting a CR2032 coin battery, be sure that the positive side is facing the locking clip. The pinouts of the CMOS battery slot are shown below.

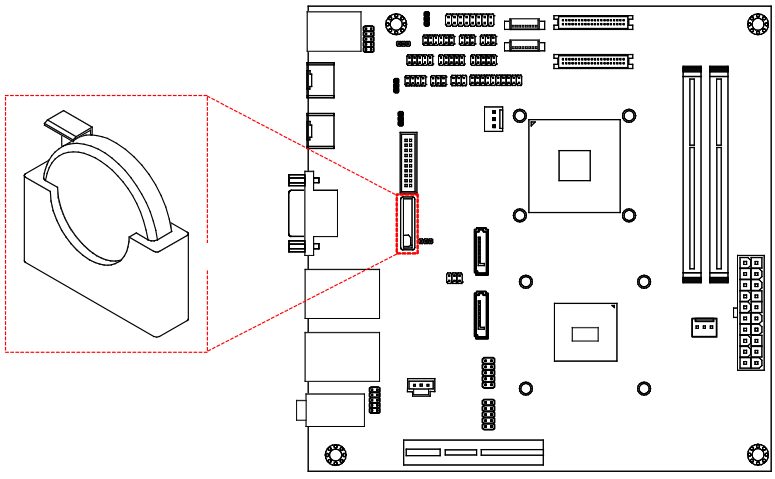

Figure 31: CMOS battery slot diagram

Pin	Signal
1	GND
2	+3V

Table 28: CMOS battery slot pinouts

2.2.18. USB 3.0 Connector

The VIA EPIA-M920 has onboard USB 3.0 connector that enables additional USB 3.0 port. The connector is labeled as "J8". The pinouts of the USB 3.0 connector are shown below.

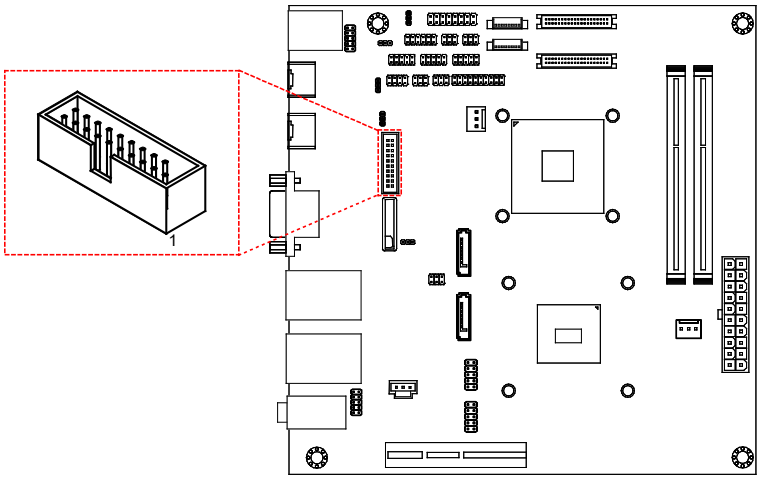

Figure 32: USB 3.0 connector diagram

Pin	Signal
1	-USBH OC8
2	USBSSRX_N2
3	USBSSRX_P2
4	GND
5	USBSSTX_N2
6	USBSSTX_P2
7	GND
8	USBHP_N8
9	USBHP_P8
10	-
11	-
12	-
13	GND
14	-
15	-
16	GND
17	-
18	-
19	+5VSUS

Table 29: USB 3.0 connector pinouts

3. Onboard Jumpers

This section will explain how to configure the VIA EPIA-M920 to match the needs of your application by setting the jumpers.

Jumper Description

A jumper consists of a pair conductive pins used to close in or bypass an electronic circuit to set up or configure a particular feature using a jumper cap. The jumper cap is a small metal clip covered by plastic. It performs like a connecting bridge to short (connect) the pair of pins. The usual colors of the jumper cap are black/red/blue/white/yellow.

Jumper Setting

There are two settings of the jumper pin: **"Short** and **Open"**. The pins are **"Short"** when a jumper cap is placed on the pair of pins. The pins are **"Open"** if the jumper cap is removed.

In addition, there are jumpers that have three or more pins, and some pins are arranged in series. In case of a jumper with three pins, place the jumper cap on pin 1 and pin 2 or pin 2 and 3 to Short it.

Some jumpers size are small or mounted on the crowded location on the board that makes it difficult to access. Therefore, using a long-nose plier in installing and removing the jumper cap is very helpful.

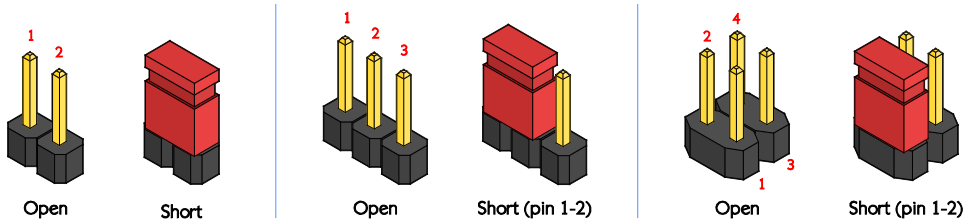

Figure 33: Jumper settings example

Caution:

Make sure to install the jumper cap on the correct pins. Installing it in the wrong pins might cause damage and malfunction.

3.1. Clear CMOS Jumper

The VIA EPIA-M920 comes with a Clear CMOS jumper. The onboard CMOS RAM stores system configuration data and has an onboard battery power supply. To reset the CMOS settings, set the jumper on pins 2 and 3 while the system is off, then return the jumper to pins 1 and 2 afterwards. Setting the jumper while the system is on will damage the board. The default setting is "Short" pins 1 and 2.

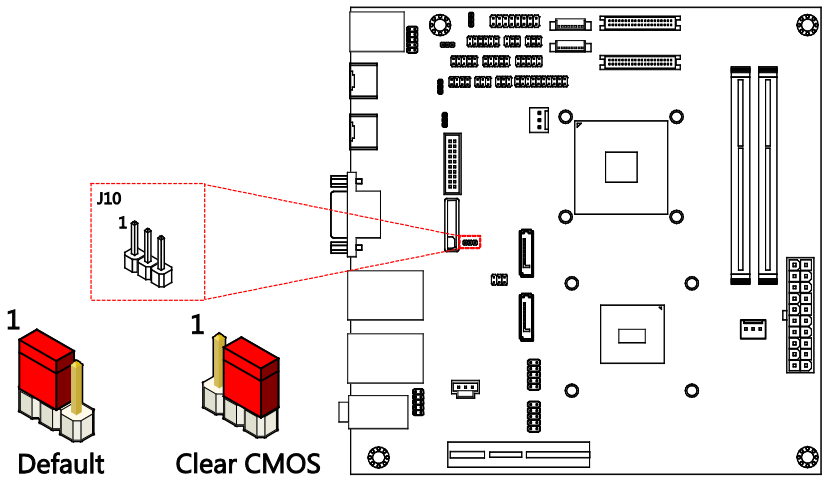

Figure 34: Clear CMOS jumper diagram

Settings	Pin 1	Pin 2	Pin 3
Regular (default)	Short	Short	Open
Clear CMOS	Open	Short	Short

Table 30: Clear CMOS jumper settings

Note:
Except when clearing the RTC RAM, never remove the cap from the Clear CMOS jumper default position. Removing the cap will cause system boot failure. Avoid clearing the CMOS while the system is on; it will damage the board.

3.2. SATA DOM Power Jumper

The SATA connectors can be used to support Disk-on-Module flash drives. The power for SATA DOM is controlled by the jumper labeled as "J12". When the jumpers are set, +5V will be delivered to the 7th pin of the SATA connectors. The jumper settings are shown below.

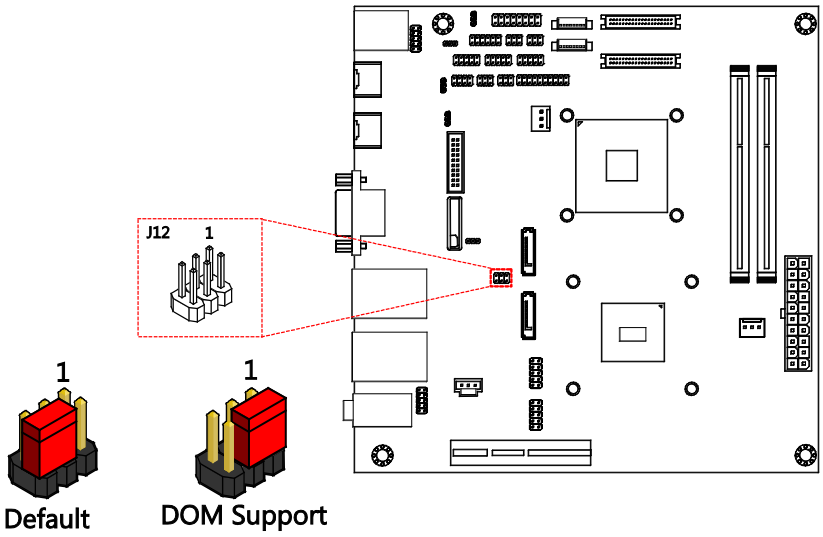

Figure 35: SATA DOM power jumper diagram

SATA1 Settings	Pin 2	Pin 4	Pin 6
DOM support	Short	Short	Open
Regular (default)	Open	Short	Short

SATA2 Settings	Pin 1	Pin 3	Pin 5
DOM support	Short	Short	Open
Regular (default)	Open	Short	Short

Table 31: SATA DOM power jumper settings

3.3. COM1 and COM2 Voltage Jumper

The voltage for COM1 and COM2 is controlled by the jumper labeled as "J11". The voltage can be either +5V or +12V. +5V is the default setting. The odd pin numbers correspond to COM1. The even pin numbers correspond to COM2. The jumper settings are shown below.

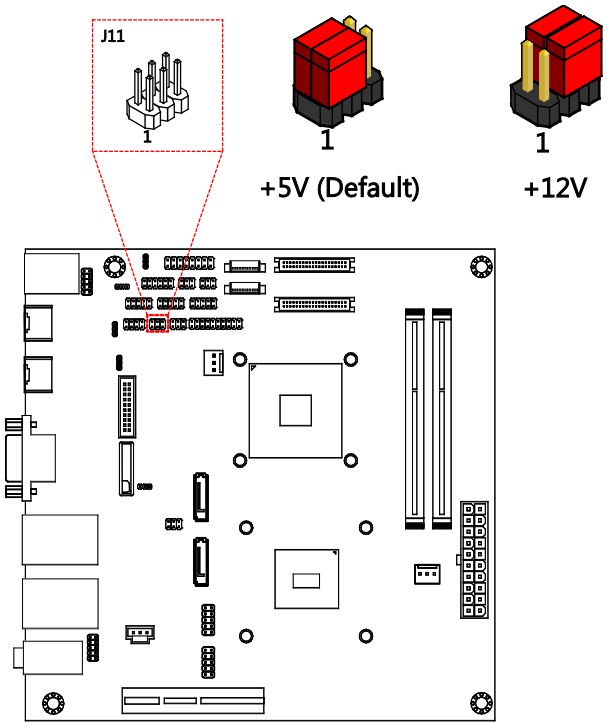

Figure 36: COM1 and COM2 voltage jumper diagram

COM1 Settings	Pin 1	Pin 3	Pin 5
+5V (default)	Short	Short	Open
+12V	Open	Short	Short

COM2 Settings	Pin 2	Pin 4	Pin 6
+5V (default)	Short	Short	Open
+12V	Open	Short	Short

Table 32: COM1 and COM2 voltage jumper settings

3.4. COM3 and COM4 Voltage Jumper

The voltage for COM3 and COM4 is controlled by the jumper labeled as "J13". The voltage can be either +5V or +12V. +5V is the default setting. The odd pin numbers correspond to COM3. The even pin numbers correspond to COM4. The jumper settings are shown below.

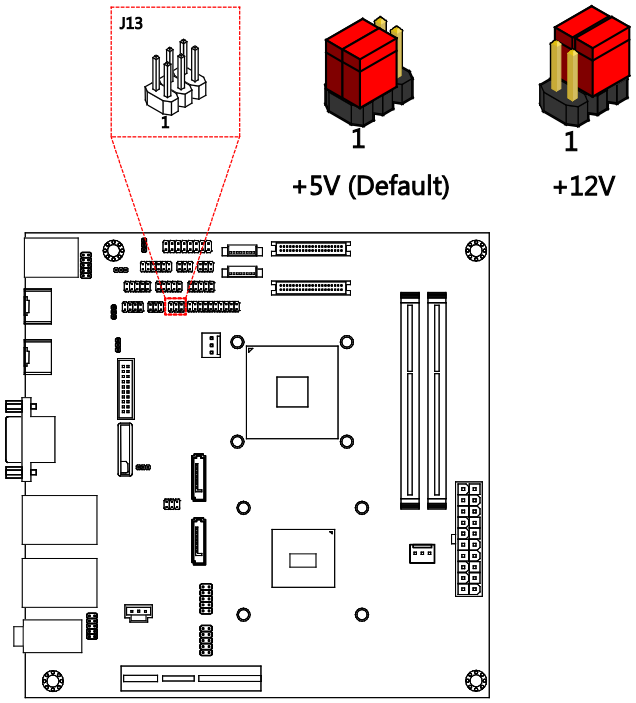

Figure 37: COM3 and COM4 voltage jumper diagram

COM3 Settings	Pin 2	Pin 4	Pin 6
+5V (default)	Short	Short	Open
+12V	Open	Short	Short

COM4 Settings	Pin 1	Pin 3	Pin 5
+5V (default)	Short	Short	Open
+12V	Open	Short	Short

Table 33: COM3 and COM4 voltage jumper settings

3.5. SPI Address Jumper

Selection of address for SPI pin header is controlled by the jumper "J6". The jumper settings are shown below.

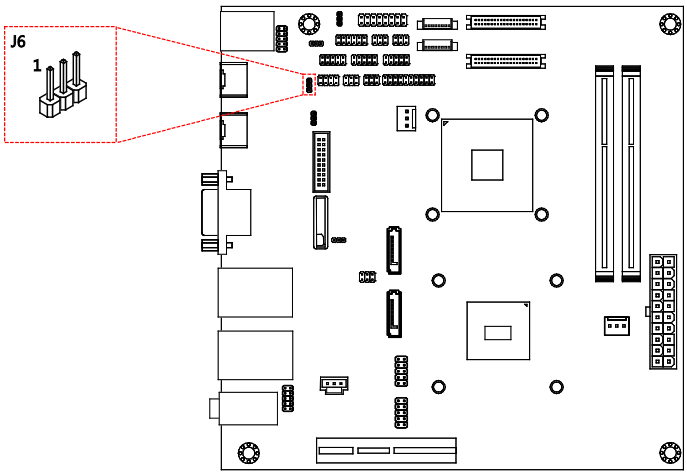

Figure 38: SPI address jumper diagram

Settings	Pin 1	Pin 2	Pin 3
MSPISS0 (default)	Short	Short	Open
MSPISS1	Open	Short	Short

Table 34: SPI address jumper settings

3.6. VDD Power Jumper

Selection of VDD power is controlled by the jumper "J9". The jumper settings are shown below.

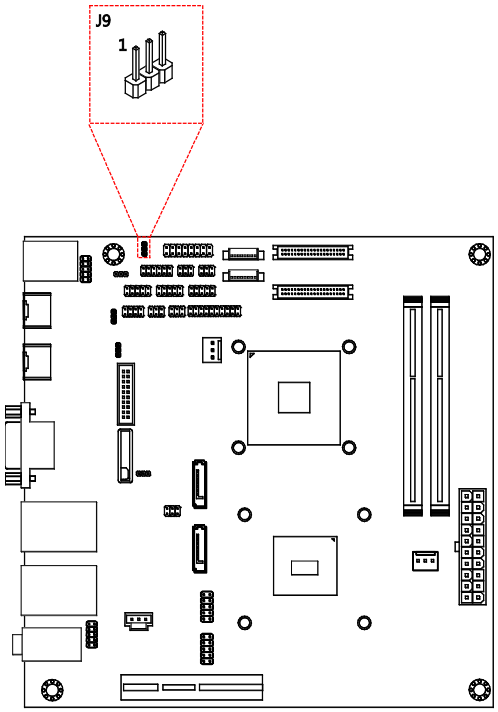

Figure 39: VDD power jumper diagram

Settings	Pin 1	Pin 2	Pin 3
VDD = 1.0V	Open	Open	Open
VDD = 0.9V	Short	Short	Open
VDD control by MPSVID (default)	Open	Short	Short

Table 35: VDD power jumper settings

3.7. LVDS1 and LVDS2 Power Jumper

The LVDS panel connectors (LVDS1 and LVDS2) and backlight control connectors (INVERTER1 and INVERTER2) can operate on different input voltages. The VIA EPIA-M920 has one jumper (J14) that controls the voltage delivered to the LVDS1 panel connector and input voltage delivered to the INVERTER1 connector. The VIA EPIA-M920 has one jumper (J15) that controls the voltage delivered to the LVDS2 panel connector and input voltage delivered to the INVERTER2 connector.

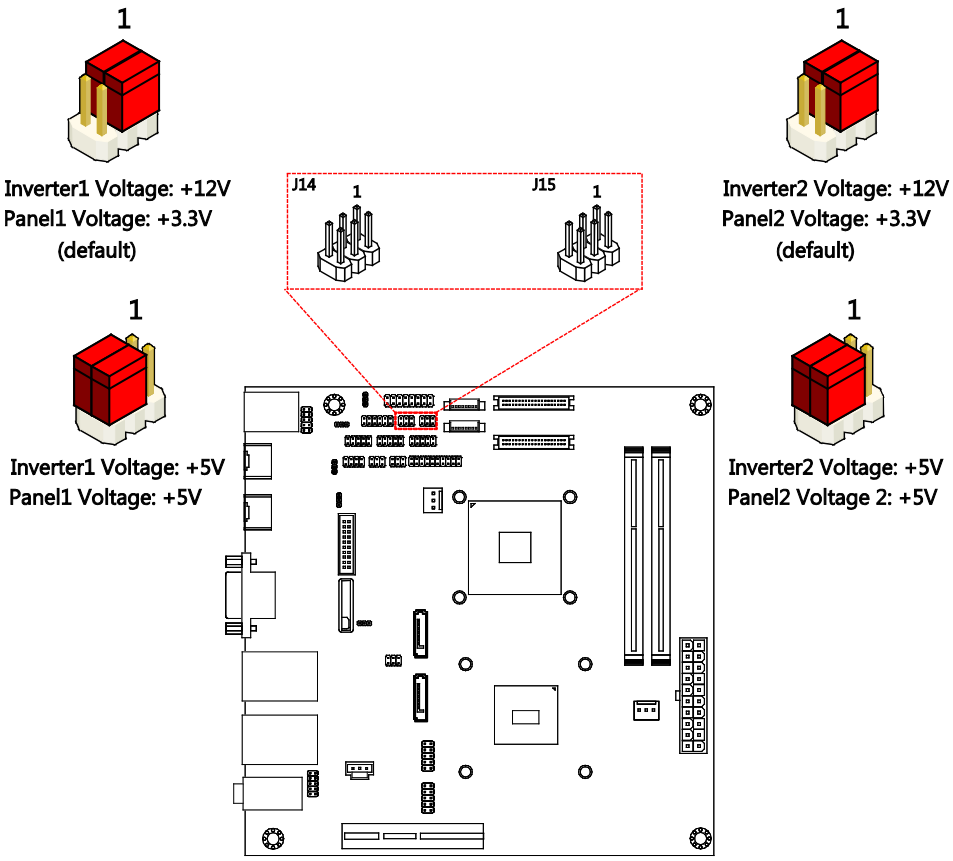

Figure 40: LVDS1 and LVDS2 power jumper diagrams

LVDS1 power jumper (J14)			
Inverter1 Settings	Pin 1	Pin 3	Pin 5
+12V (default)	Short	Short	Open
+5V	Open	Short	Short
LVDS1 panel Settings	Pin 2	Pin 4	Pin 6
+3.3V (default)	Short	Short	Open
+5V	Open	Short	Short

LVDS2 power jumper (J15)			
Inverter2 Settings	Pin 1	Pin 3	Pin 5
+12V (default)	Short	Short	Open
+5V	Open	Short	Short
LVDS2 panel Settings	Pin 2	Pin 4	Pin 6
+3.3V (default)	Short	Short	Open
+5V	Open	Short	Short

Table 36: LVDS1 and LVDS2 power jumper settings

3.8. DDR3 SODIMM Voltage Jumper

The selection of the voltage input for the DDR3 SODIMM memory is controlled by the jumper "J16". The jumper settings are shown below.

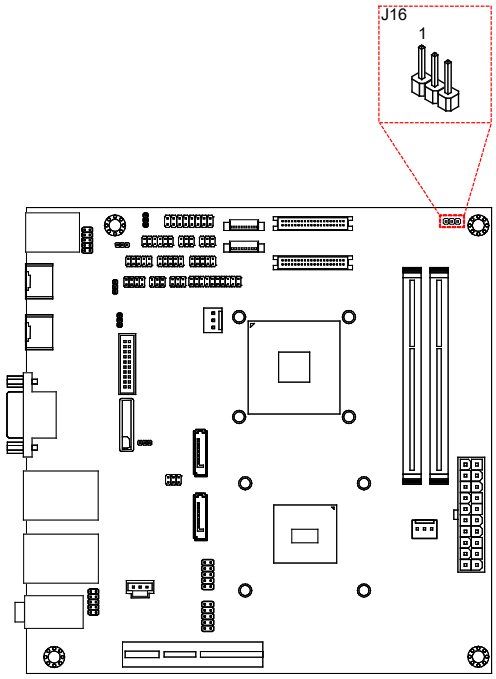

Figure 41: DDR3 SODIMM voltage jumper diagram

Settings	Pin 1	Pin 2	Pin 3
+1.5V (default)	Short	Short	Open
+1.35V	Open	Short	Short

Table 37: DDR3 SODIMM voltage jumper settings

4. Expansion Slots

4.1. DDR3 Memory Slots

The VIA EPIA-M920 provides two DDR3 SODIMM memory slots. The memory slot can accommodate up to 8GB of 1333MHz memory per slot. The memory slots are labeled as "SODIMM1" and "SODIMM2". The location of the DDR3 memory slots are shown below.

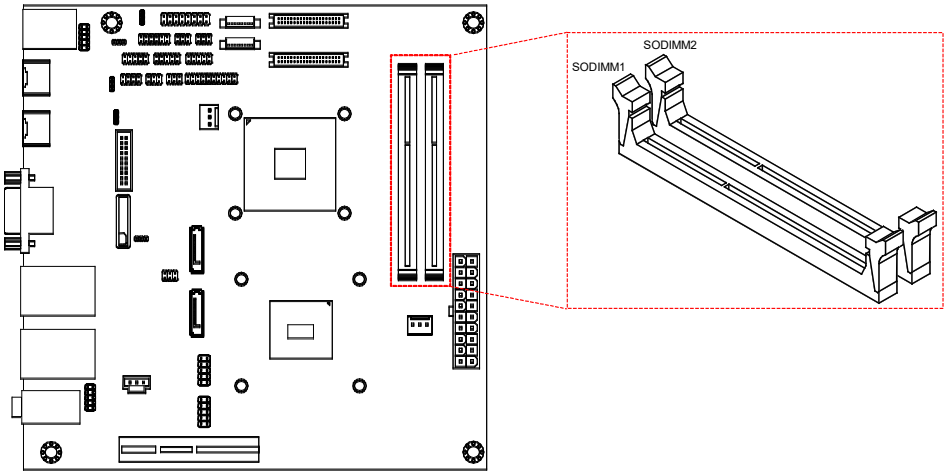

Figure 42: DDR3 memory slots diagram

4.1.1. Installing a Memory Module

Step 1

Disengage the locking clasps at both ends of the memory slot. Align the notch on the bottom of the SODIMM memory module with the notch wedge in the slot.

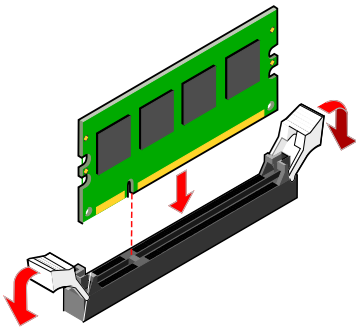

Figure 43: Inserting the memory module

Step 2

Slide the SODIMM memory module into the side grooves and push the module into the slot until the locking clasps snap into the closed position.

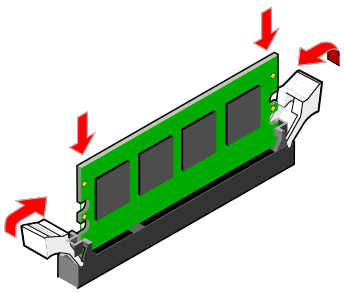

Figure 44: Locking the memory module

4.1.2. Removing a Memory Module

Step 1

Disengage the locking clips at both ends of the memory slot.

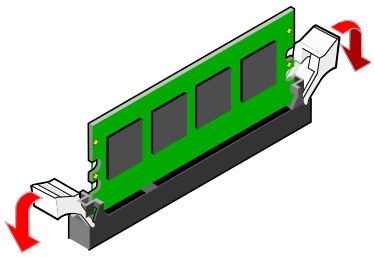

Figure 45: Disengaging the locking clips

Step 2

When the locking clips have been cleared, the SODIMM memory module will automatically pop up. Remove the memory module.

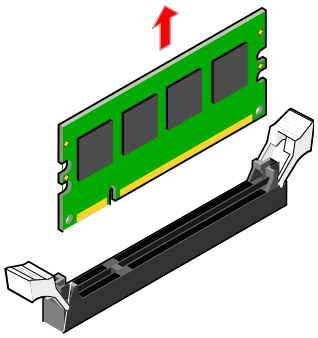

Figure 46: Removing the memory module

4.2. PCI Express Slot

The PCI Express slot provides support for 4-lane cards. Due to the orientation of the slot, a riser card module[1] must be used. The location of the PCI Express slot is shown below.

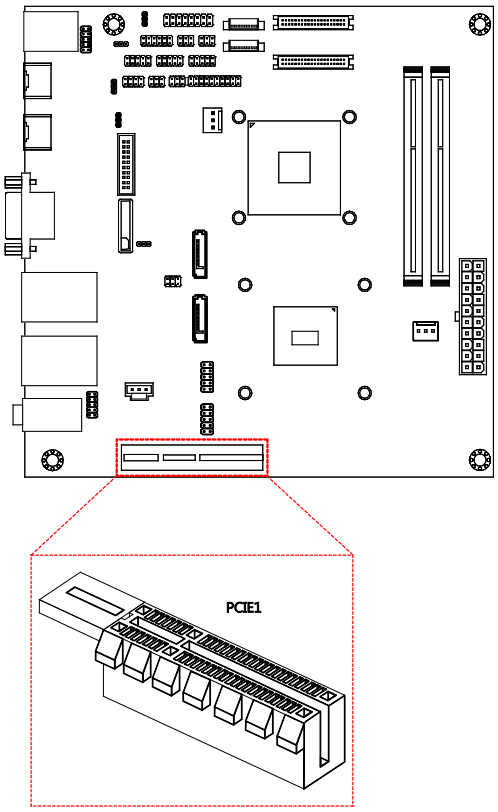

Figure 47: PCI Express slot diagram

Note:
1. The optional riser card is PCIE-03.

5. Hardware Installation

5.1. Installing into a Chassis

The VIA EPIA-M920 can be fitted into any chassis that has mounting holes for compatible with the standard Mini-ITX mounting hole locations. Additionally, the chassis must meet the minimum height requirements for specified areas of the board. If a riser card module is being used, the chassis will need to accommodate the additional space requirements.

5.1.1. Suggested Minimum Chassis Dimensions

The figure below shows the suggested minimum space requirements that a chassis should have in order to work well with the VIA EPIA-M920.

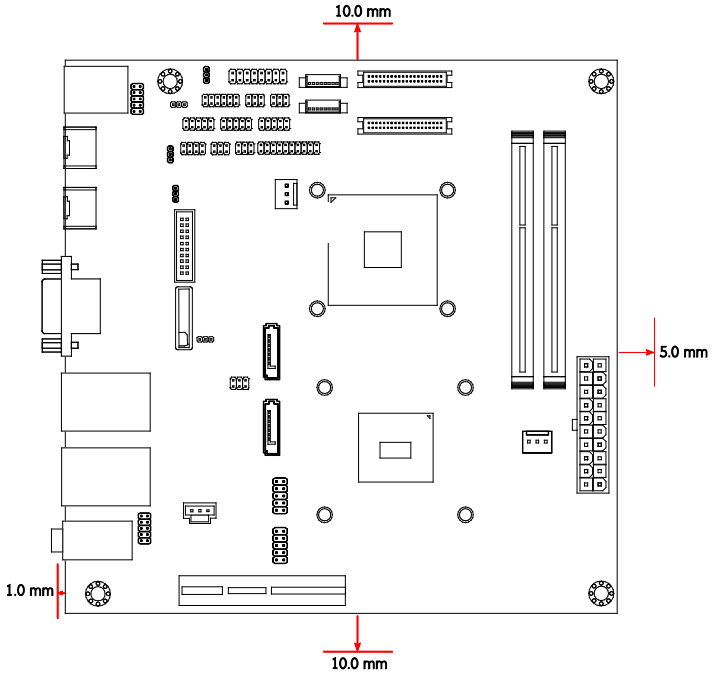

Figure 48: Suggested minimum chassis dimensions

Each side of the board should have a buffer zone from the internal wall of the chassis. The side of the board that accommodates the I/O coastline should have a buffer of 1mm. The side on the opposite end of the I/O coastline should have a buffer of at least 5mm. The two sides adjacent to the I/O coastline should have at least a 10mm buffer.

For the side that is close to the PCIe slot, the buffer should be at least 100mm if a riser card will be used.

5.1.2. Suggested Minimum Chassis Height

The figure below shows the suggested minimum height requirements for the internal space of the chassis. It is not necessary for the internal ceiling to be evenly flat. What is required is that the internal ceiling height must be strictly observed for each section that is highlighted. The highest part of the ceiling will be above the PCIe slot.

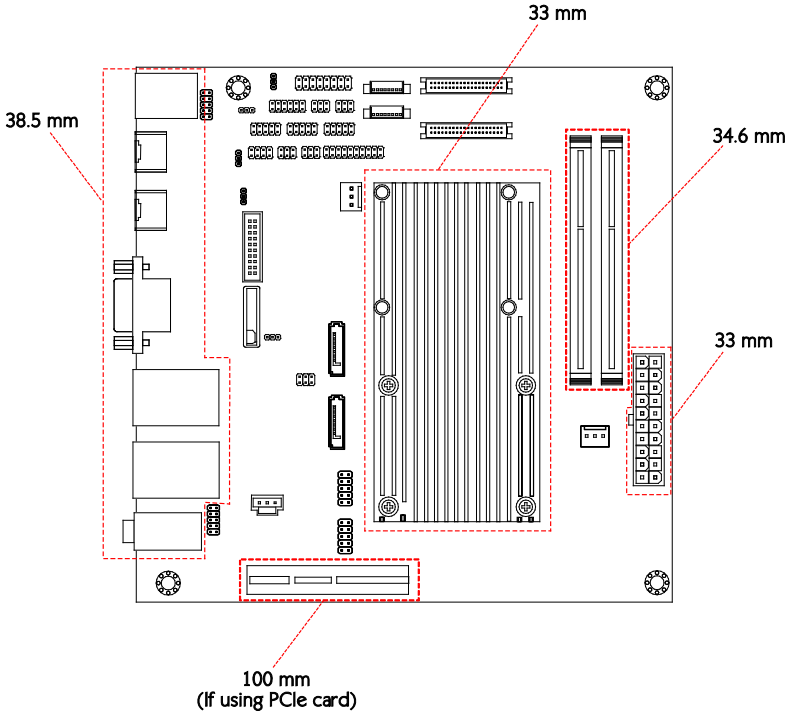

Figure 49: Suggested minimum internal chassis ceiling height (for fanless model)

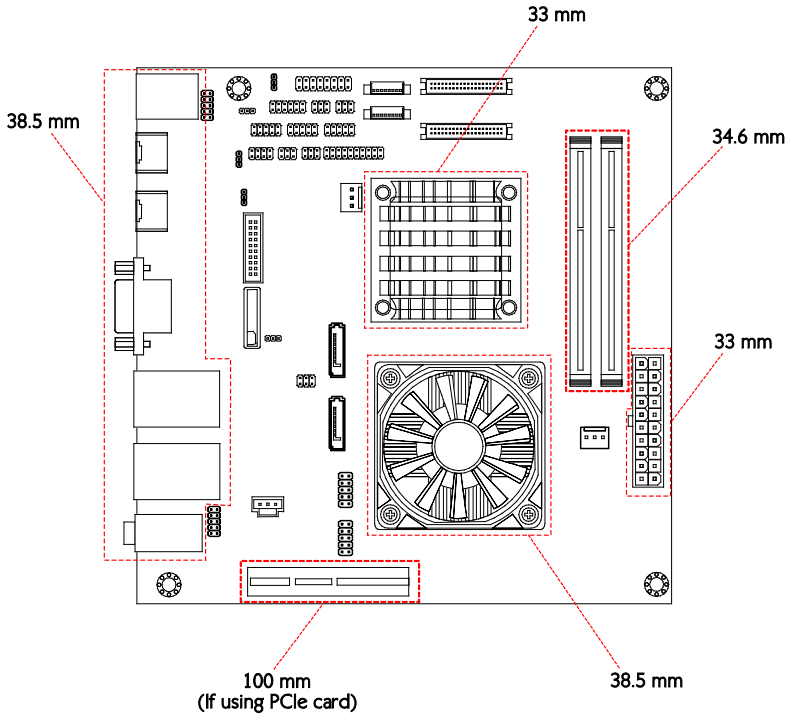

Figure 50: Suggested minimum internal chassis ceiling height (for fan model)

5.1.3. Suggested Keepout Areas

The figure below shows the areas of the board that we recommend should be left unobstructed.

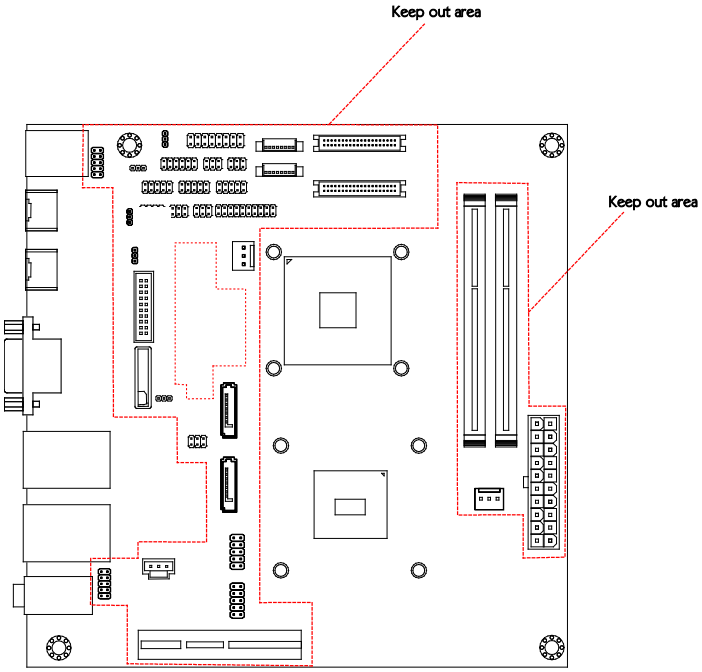

Figure 51: Suggested keepout areas

6. BIOS Setup Utility

6.1. Entering the BIOS Setup Utility

Power on the computer and press **Delete** during the beginning of the boot sequence to enter the BIOS Setup Utility. If the entry point has passed, restart the system and try again.

6.2. Control Keys

Up Move up one row

Down Move down one row

Left Move to the left in the navigation bar

Right Move to the right in the navigation bar

Enter Access the highlighted item / Select the item

Esc Jumps to the Exit screen or returns to the previous screen

Page up / +[1] Increase the numeric value

Page down / -[1] Decrease the numeric value

F1 General help[2]

F2 Restore the previous CMOS value

F3 Load optimized defaults

F4 Save all the changes and exit

Notes:
1. Must be pressed using the 10-key pad.
2. The General help contents are only for the Status Page and Option Page setup menus.

6.3. Navigating the BIOS Menus

The main menu displays all the BIOS setup categories. Use the <**Left**>/<**Right**> and <**Up**>/<**Down**> arrow keys to select any item or sub-menu. Descriptions of the selected/highlighted category are displayed at the bottom of the screen.

The small triangular arrowhead symbol next to a field indicates that a sub-menu is available (see figure below). Press <**Enter**> to display the sub-menu. To exit the sub-menu, press <**Esc**>.

6.4. Getting Help

The BIOS Setup Utility provides a "**General Help**" screen. This screen can be accessed at any time by pressing **F1**. The help screen displays the keys for using and navigating the BIOS Setup Utility. Press **Esc** to exit the help screen.

6.5. Main Menu

The System Overview screen is the default screen that is shown when the BIOS Setup Utility is launched. This screen can be accessed by traversing the navigation bar to the "Main" label.

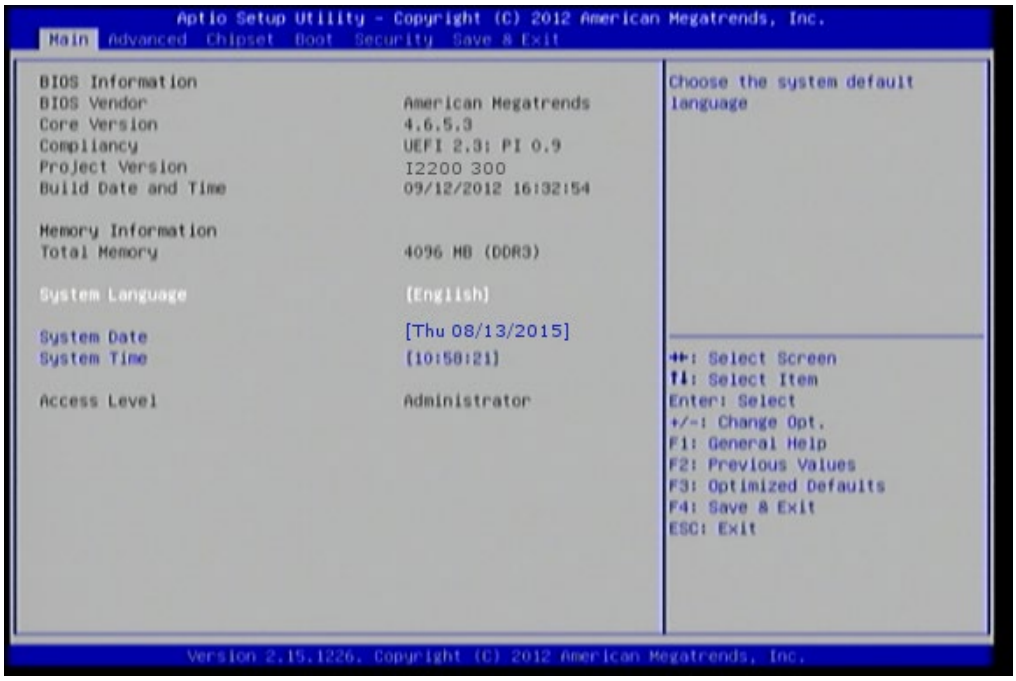

Figure 52: Illustration of the Main menu screen

6.5.1. BIOS Information

The content in this section of the screen shows the information about the vendor, the Core version, UEFI specification version, the project version and date & time of the project build.

6.5.2. Memory Information

This section shows the amount of memory that is installed on the hardware platform.

6.5.3. System Language

This option allows the user to configure the language that the user wants to use.

6.5.4. System Date

This section shows the current system date. Press **Tab** to traverse right and **Shift+Tab** to traverse left through the month, day, and year segments. The **+** and **-** keys on the number pad can be used to change the values. The weekday name is automatically updated when the date is altered. The date format is [Weekday, Month, Day, Year].

6.5.5. System Time

This section shows the current system time. Press **Tab** to traverse right and **Shift+Tab** to traverse left through the hour, minute, and second segments. The **+** and **-** keys on the number pad can be used to change the values. The time format is [Hour : Minute : Second].

6.6. Advanced Settings

The Advanced Settings screen shows a list of categories that can provide access to a sub-screen. Sub-screen links can be identified by the preceding right-facing arrowhead.

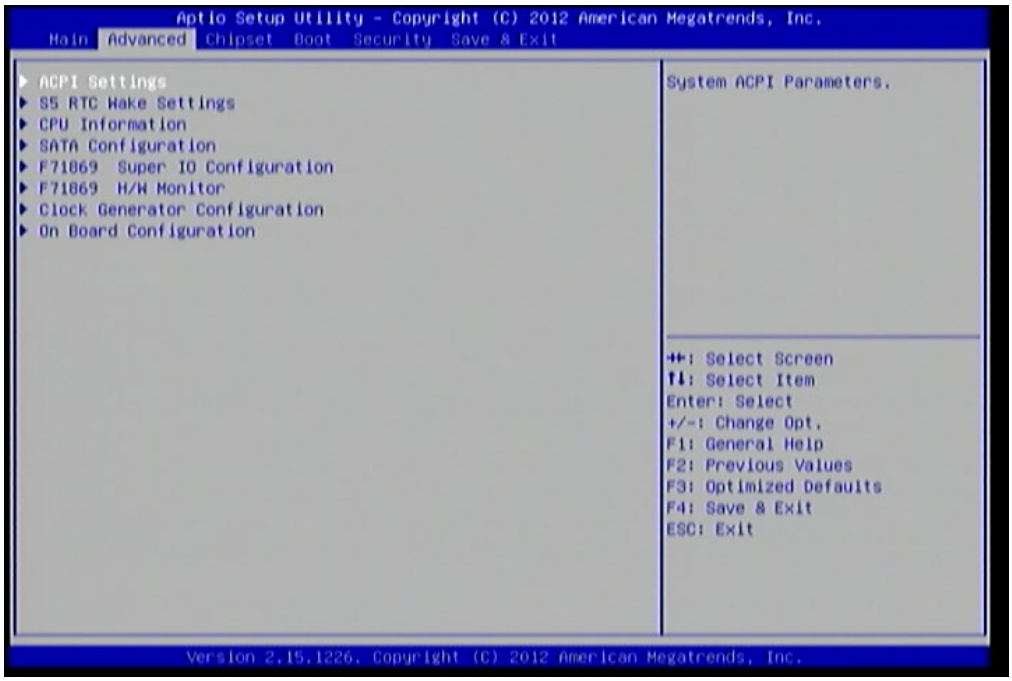

Figure 53: Illustration of the Advanced Settings screen

The Advanced Settings screen contains the following links:

- ACPI Settings
- S5 RTC Wake Settings
- CPU Information
- SATA Configuration
- F71869 Super IO Configuration
- F71869 H/W Monitor
- Clock Generator Configuration
- On Board Configuration

6.6.1. ACPI Settings

ACPI grants the operating system direct control over system power management. The ACPI Configuration screen can be used to set a number of power management related functions.

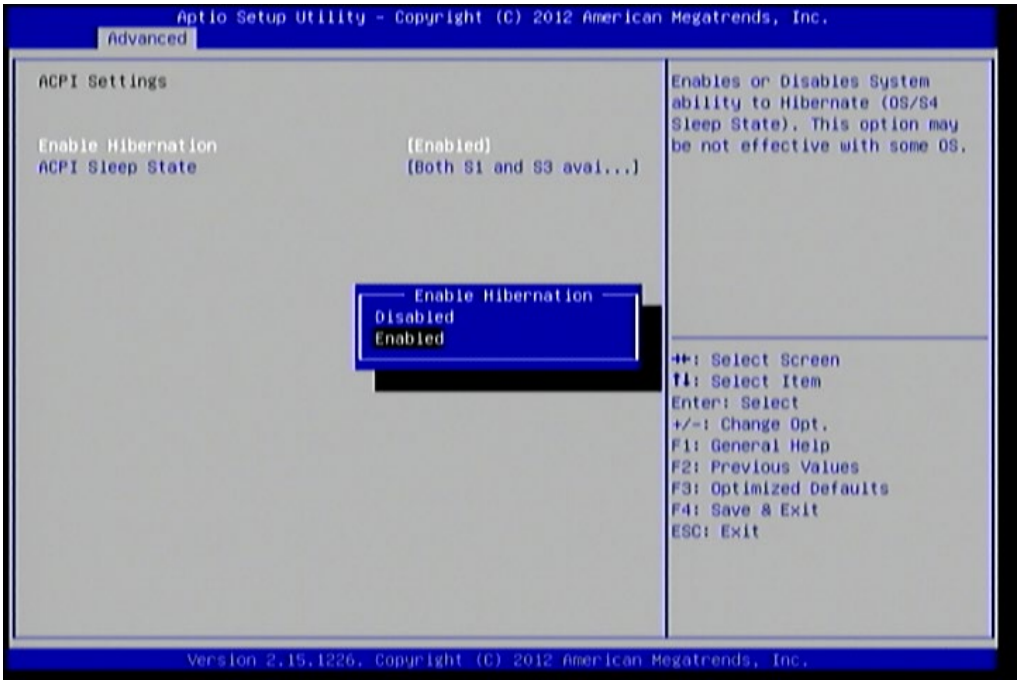

Figure 54: Illustration of the ACPI Settings screen

6.6.1.1. Enable Hibernation

Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

6.6.1.2. ACPI Sleep State

Select ACPI sleep state the system will enter when the SUSPEND button is pressed. Available options are: Suspend Disabled/S1 only (CPU Stop Clock)/S3 only (Suspend to RAM)/Both S1 and S3 available for OS to choose from.

6.6.2. S5 RTC Wake Settings

Enable system to wake from S5 using RTC alarm.

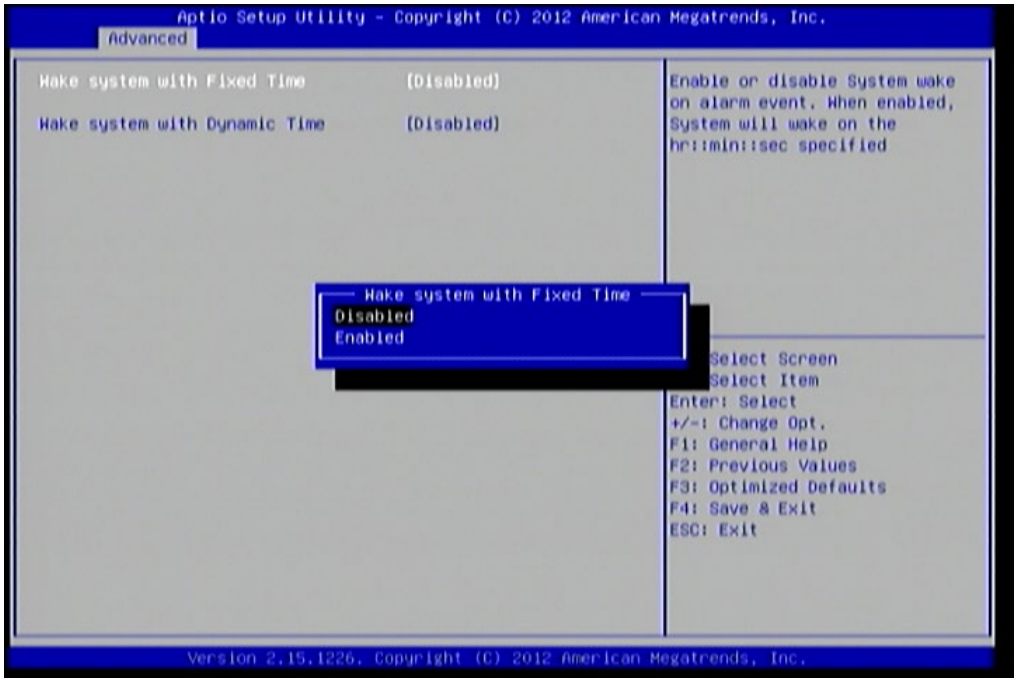

Figure 55: Illustration of S5 RTC Wake Settings screen

6.6.2.1. Wake system with Fixed Time

This feature has two options: Enable or Disable system wake on alarm event. When enabled, system will wake on the hr:min:sec specified.

6.6.2.2. Wake system with Dynamic Time

This feature has two options: Enable or Disable system wake on alarm event. When enabled, system will wake on the current time + increase minute(s).

6.6.3. CPU Information

The CPU Information screen shows detailed information about the built-in processor.

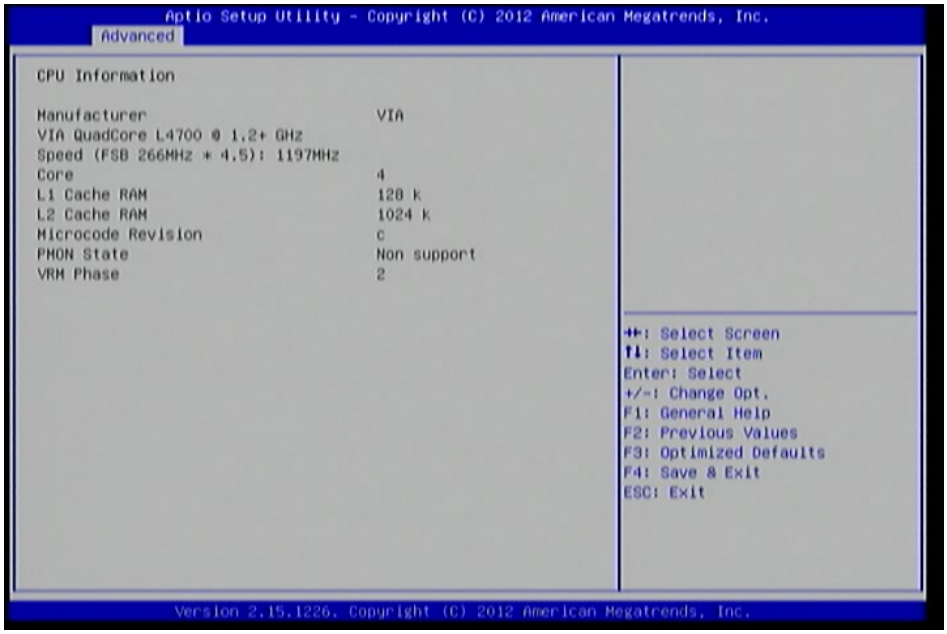

Figure 56: Illustration of CPU Information screen

6.6.4. SATA Configuration

The SATA Configuration screen allows the user to view and configure the settings of the SATA configuration settings.

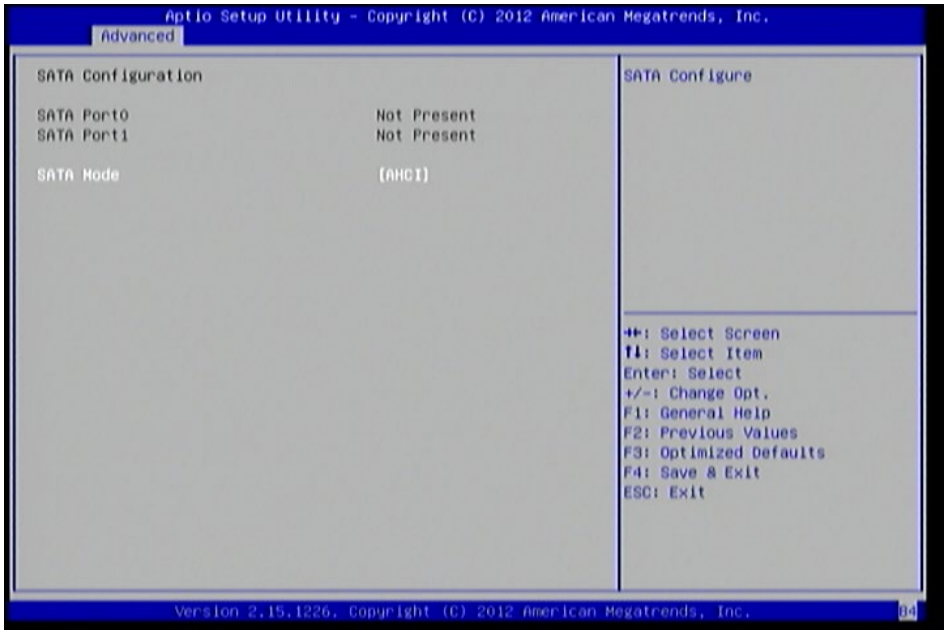

Figure 57: Illustration of SATA Configuration screen

6.6.4.1. SATA Mode

This option allows the user to manually configure SATA controller for a particular mode.

IDE Mode
Set this value to change the SATA to IDE mode.

AHCI Mode
Set this value to change the SATA to AHCI mode.

6.6.5. F71869 Super IO Configuration

The F71869 Super IO Configuration screen allows the user to set system Super IO Chip parameters.

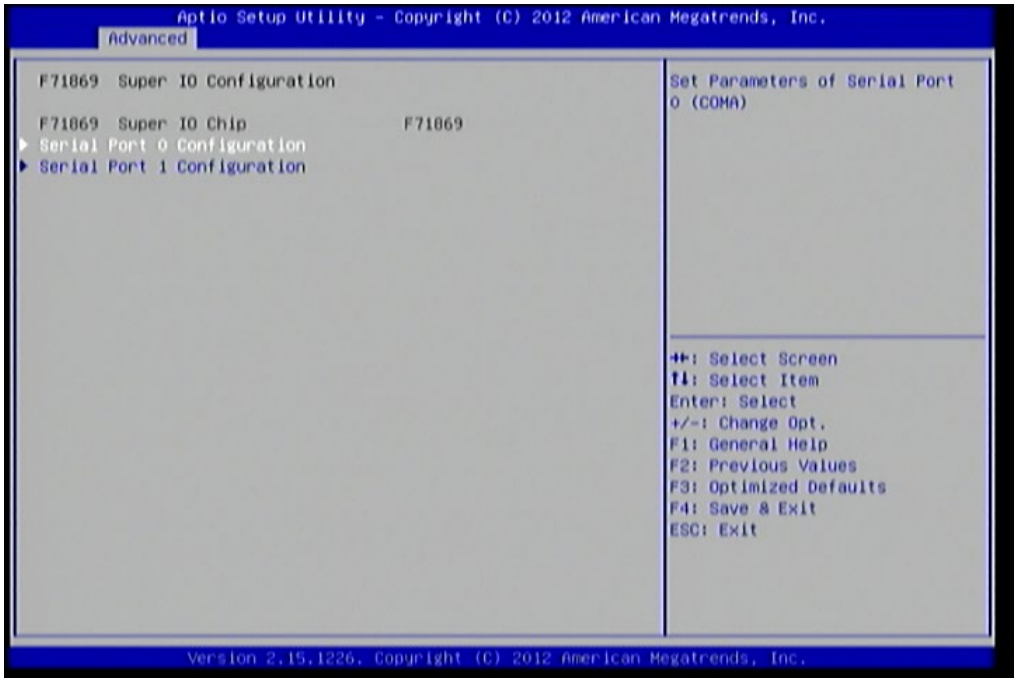

Figure 58: Illustration of F71869 Super IO Configuration screen

6.6.5.1. Serial Port 0 Configuration

Set parameters of Serial Port 0 (COMA).

6.6.5.1.1. Serial Port

This feature has two options: Enable or Disable Serial Port (COM).

6.6.5.2. Serial Port 1 Configuration

Set parameters of Serial Port 1 (COMB)

6.6.5.2.1. Serial Port

This feature has two options: Enable or Disable Serial Port (COM).

6.6.5.2.2. Device Mode

Change the Serial Port mode. Select <High Speed> or <Normal Mode> mode.

6.6.6. F71869 H/W Monitor

F71869 H/W Monitor shows Monitor hardware status.

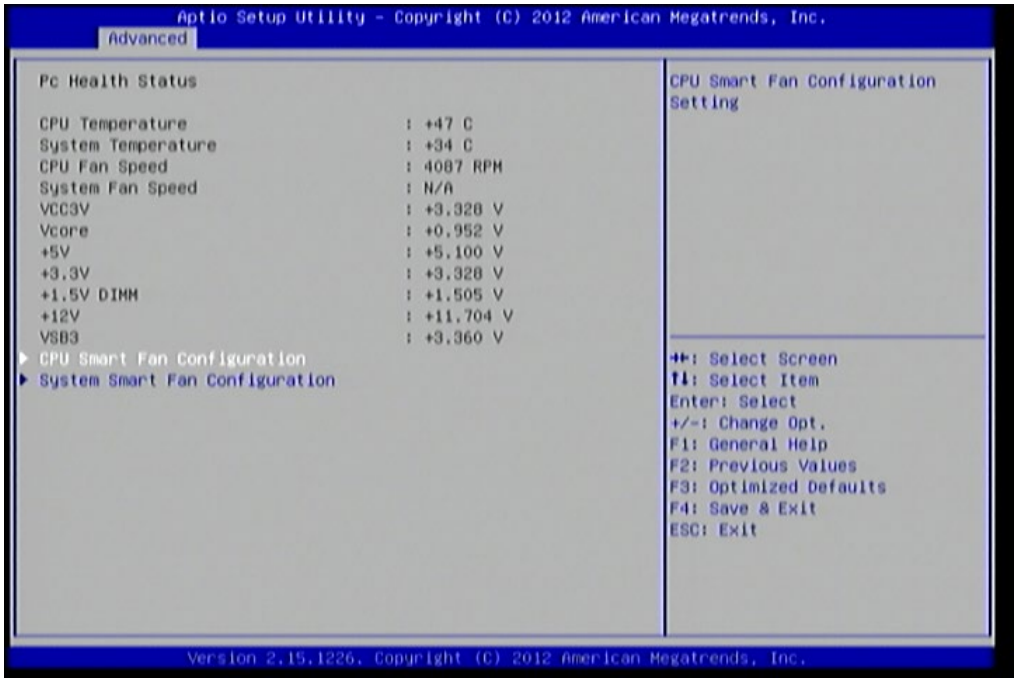

Figure 59: Illustration of F71869 H/W Monitor screen

6.6.6.1. CPU Smart Fan Configuration

CPU Smart Fan Configuration Setting

6.6.6.1.1. Smart Fan Support

This feature has two options: Enable or Disable Smart Fan.

6.6.6.2. System Smart Fan Configuration

System Smart Fan Configuration Setting

6.6.6.2.1. Smart Fan Support

This feature has two options: Enable or Disable Smart Fan.

6.6.7. Clock Generator Configuration

The Clock Generator Configuration screen enables access to the Spread Spectrum Setting feature.

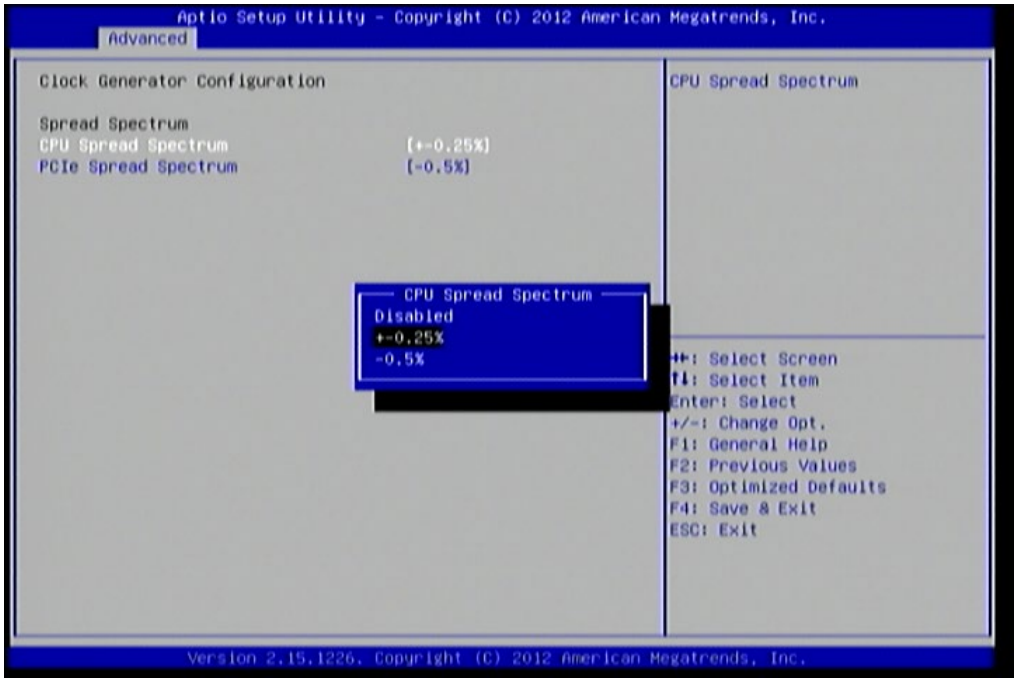

Figure 60: Illustration of Clock Generator Configuration screen

6.6.7.1. CPU Spread Spectrum

The Spread Spectrum Setting feature enables the BIOS to modulate the clock frequencies originating from the board. The settings are in percentages of modulation. Higher percentages result in greater modulation of clock frequencies. This feature has 3 options: Disable, +-0.25% and -0.5%.

6.6.7.2. PCIe Spread Spectrum

Select PCIe Spread Spectrum. This feature has two options: Disable and -0.5%.

6.6.8. OnBoard Configuration

The OnBoard Device Configuration screen has the following features.

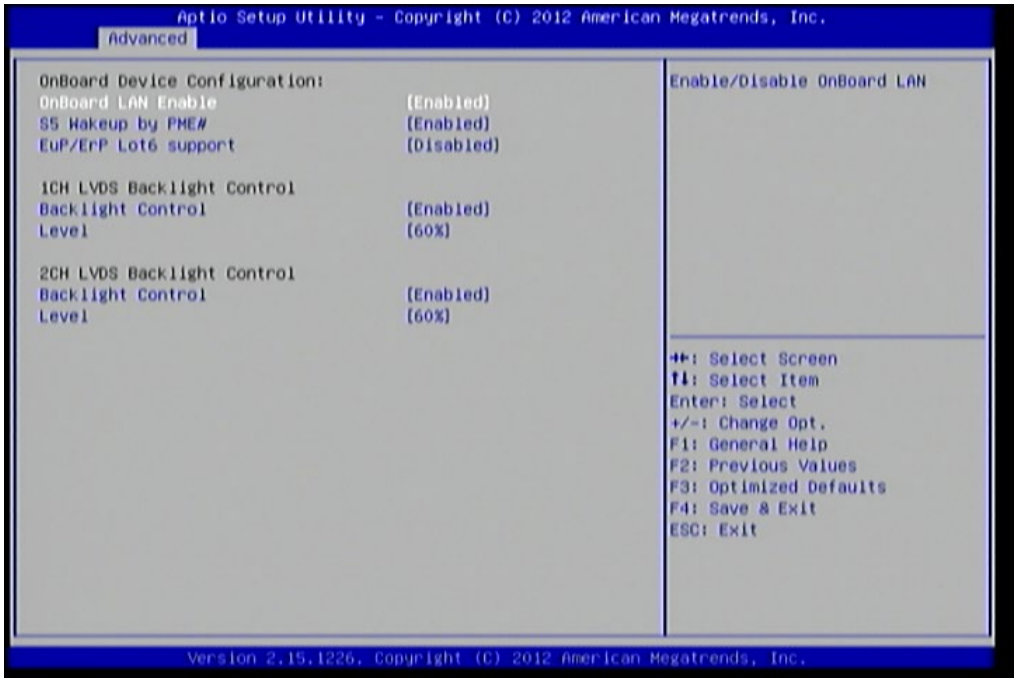

Figure 61: Illustration of OnBoard Configuration screen

OnBoard Device Configuration:

6.6.8.1. OnBoard LAN Enable

The OnBoard LAN Enable feature determines whether the onboard LAN controller will be used or not.

6.6.8.2. S5 Wakeup by PME#

The S5 Wakeup by PME# feature enables the BIOS to allow remote wake-up from the S5 power off state through the PCI bus.

6.6.8.3. EuP/ErP Lot6 support

The EuP/ErP Lot6 Support feature enables the BIOS to reduce the power draw to less than 1W when the system is in standby mode. This feature has two options: enabled and disabled.

6.6.8.4. 1CH LVDS Backlight Control

Backlight Control

The Backlight Control feature control by VX11H enables the user to control the brightness of the 1CH LVDS backlight. This feature has six options.

Level

0%, 20%, 40%, 60%, 80% and 100%.

6.6.8.5. 2CH LVDS Backlight Control

Backlight Control

The Backlight Control feature control by VX11H enables the user to control the brightness of the 2CH LVDS backlight. This feature has six options.

Level

0%, 20%, 40%, 60%, 80% and 100%.

6.7. Chipset Settings

The Chipset Settings screen shows a list of categories that can provide access to a sub-screen. Sub-screen links can be identified by the preceding right-facing arrowhead.

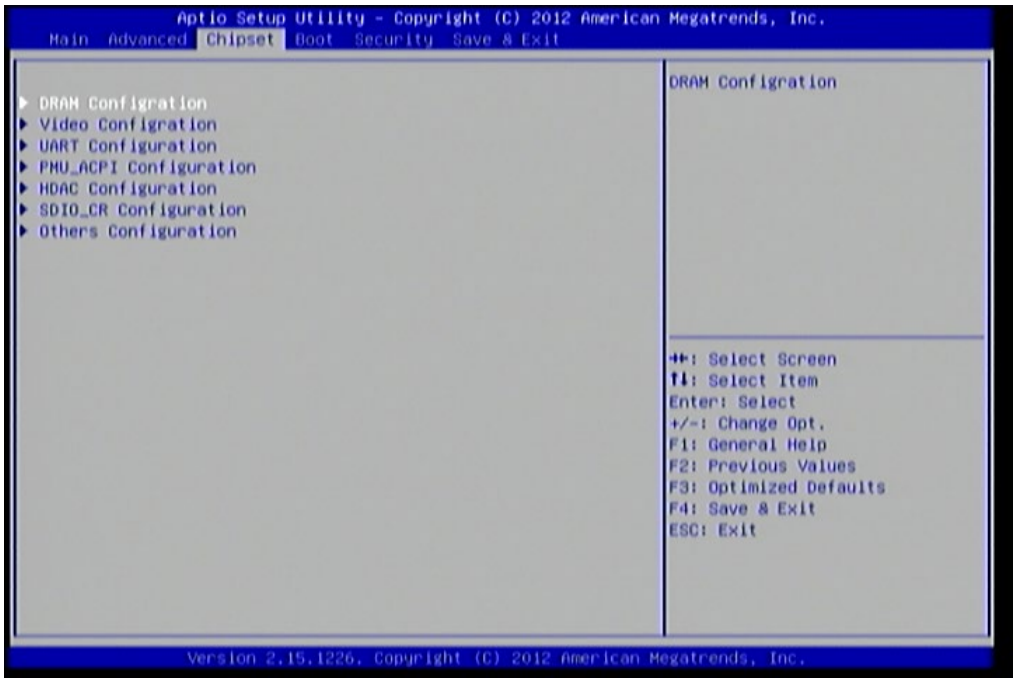

Figure 62: Illustration of Chipset Settings screen

The Chipset Settings screen contains the following links:

- DRAM Configuration
- Video Configuration
- UART Configuration
- PMU-ACPI Configuration
- HDAC Configuration
- SDIO_CR Configuration
- Others Configuration

6.7.1. DRAM Configuration

The DRAM Configuration screen has two features for controlling the system DRAM. All other DRAM features are automated and cannot be accessed.

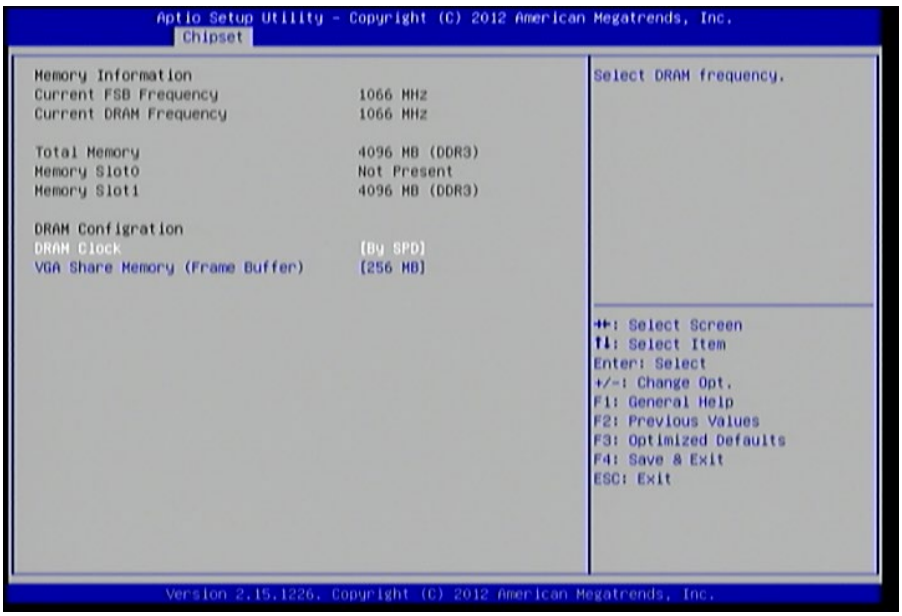

Figure 63: Illustration of DRAM Configuration screen

6.7.1.1. DRAM Clock

The DRAM Clock option enables the user to determine how the BIOS handles the memory clock frequency. The memory clock can either be dynamic or static. This feature has eleven options.

By SPD

By SPD option enables the BIOS to select a compatible clock frequency for the installed memory.

400MHz

The 400MHz option forces the BIOS to be fixed at 800MHz for DDR3 memory modules.

533MHz

The 533MHz option forces the BIOS to be fixed at 1066MHz for DDR3 memory modules.

566MHz

The 566MHz option forces the BIOS to be fixed at 1132MHz for DDR3 memory modules.

600MHz

The 600MHz option forces the BIOS to be fixed at 1200MHz for DDR3 memory modules.

633MHz

The 633MHz option forces the BIOS to be fixed at 1266MHz for DDR3 memory modules.

667MHz

The 667MHz option forces the BIOS to be fixed at 1334MHz for DDR3 memory modules.

700MHz

The 700MHz option forces the BIOS to be fixed at 1400MHz for DDR3 memory modules

733MHz

The 733MHz option forces the BIOS to be fixed at 1466MHz for DDR3 memory modules

766MHz

The 766MHz option forces the BIOS to be fixed at 1532MHz for DDR3 memory modules

800MHz

The 800MHz option forces the BIOS to be fixed at 1600MHz for DDR3 memory modules

6.7.1.2. VGA Share Memory (Frame Buffer)

The VGA Share Memory feature enables the user to choose the amount of the system memory to reserve for use by the integrated graphics controller. The selections of memory amount that can be reserved are 256MB and 512MB.

6.7.2. Video Configuration

The Video Configuration screen has features for controlling the integrated graphics controller in the VX11H chipset.

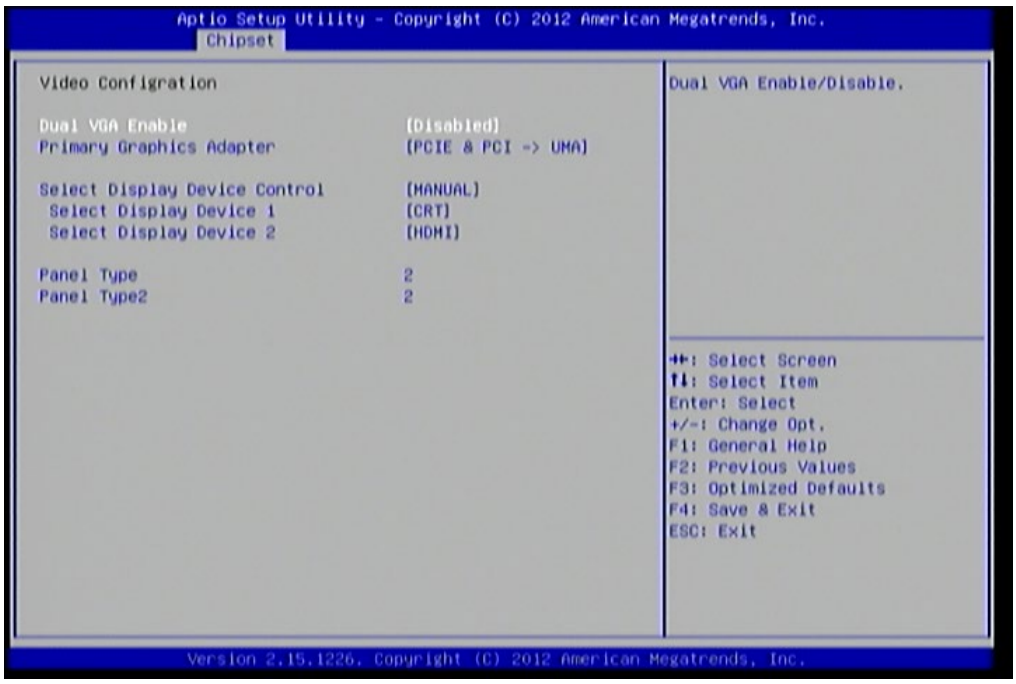

Figure 64: Illustration of Video Configuration screen

6.7.2.1. Dual VGA Enable

This feature has two options: Enable/Disable Dual VGA.

6.7.2.2. Primary Graphics Adapter

The Primary Graphics Adapter option enables the user to change the order in which the BIOS seeks for a graphics adapter. There are three paths that can be chosen.

PCIE & PCI -> UMA

UMA -> PCIE & PCI

6.7.2.3. Select Display Device Control

Available selections are: Auto and Manual.

6.7.2.4. Select Display Device 1 and 2

The Select Display Device feature enables the user to choose a specific display interface. This feature has four options: CRT, LCD, LCD2, HDMI and HDMI2. If both Select Display Device 1 and Select Display Device 2 are set to the same interface, then any display device connected to the other interface will not function. For example, if both Select Display 1 and 2 are set to CRT, then no data will be sent to the LCD, LCD2, HDMI and HDMI2 port.

6.7.2.5. Panel Type

The Panel Type feature enables the user to specify the resolution of the display being used with the system. The panel types are predefined in the VGA VBIOS.

Panel Type	Resolution
00	640 x 480
01	800 x 600
02	1024 x 768
03	1280 x 768
04	1280 x 1024
05	1400 x 1050
06	1440 x 900
07	1280 x 800

Panel Type	Resolution
08	800 x 480
09	1024 x 600
10	1366 x 768
11	1600 x 1200
12	1680 x 1050
13	1920 x 1200
14	1920 x 1080
15	1024 x 576

6.7.2.6. Panel Type2

The Panel Type feature enables the user to specify the resolution of display 2 being used with the system. The panel types are predefined in the VGA VBIOS.

Panel Type	Resolution
00	640 x 480
01	800 x 600
02	1024 x 768
03	1280 x 768
04	1280 x 1024
05	1400 x 1050
06	1440 x 900
07	1280 x 800

Panel Type	Resolution
08	800 x 480
09	1024 x 600
10	1366 x 768
11	1600 x 1200
12	1680 x 1050
13	1920 x 1200
14	1920 x 1080
15	1024 x 576

6.7.3. UART Configuration

The UART Configuration screen allows the user to set UART configuration parameters.

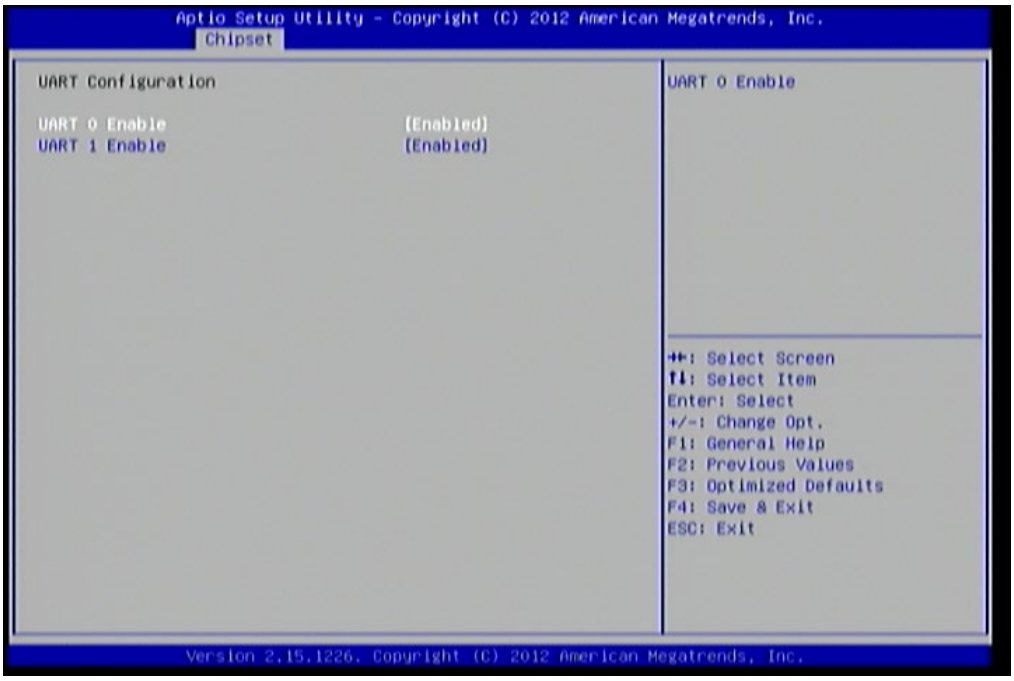

Figure 65: Illustration of UART Configuration screen

6.7.3.1. UART 0 Enable

This feature has 2 options: Enable/Disable UART 0.

6.7.3.2. UART 1 Enable

This feature has 2 options: Enable/Disable UART 1.

6.7.4. PMU_ACPI Configuration

The PMU_ACPI Configuration screen can be used to set a number of power management related functions.

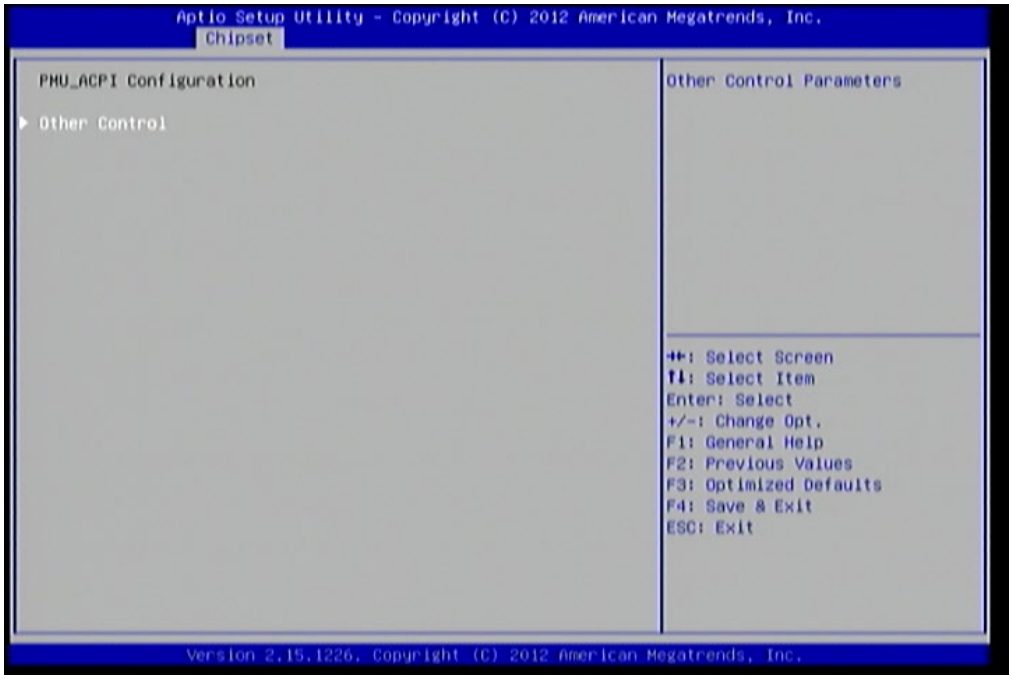

Figure 66: Illustration of PMU_ACPI Configuration screen Other Control

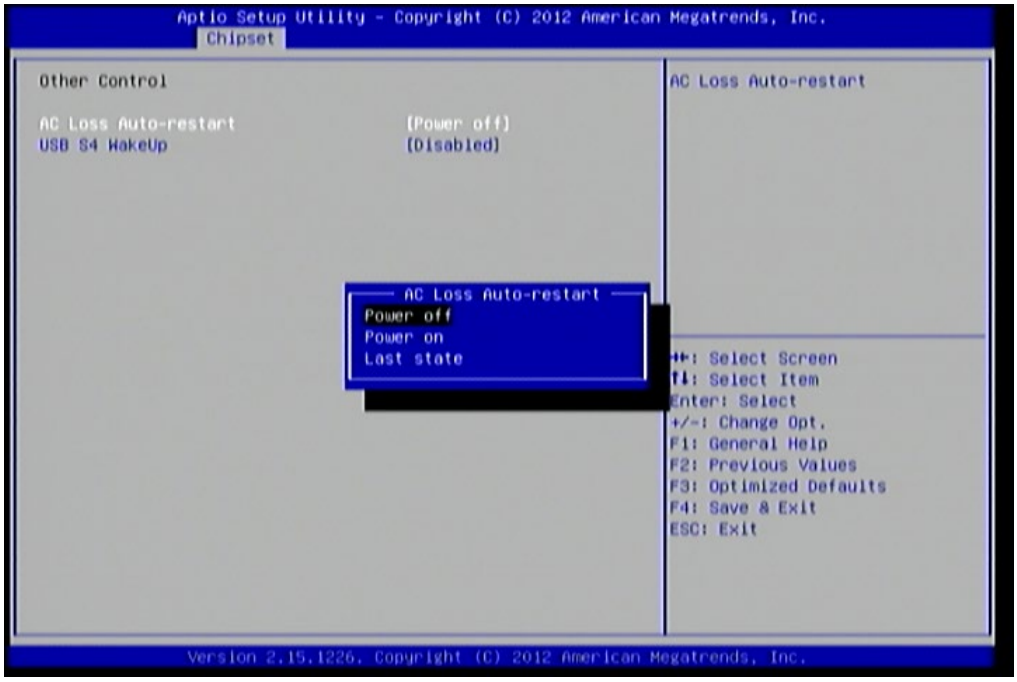

Figure 67: Illustration of Other Control screen

6.7.4.1.1. AC Loss Auto-restart

AC Loss Auto-restart defines how the system will respond after AC power has been interrupted while the system is on. There are three options.

Power Off

The Power Off option keeps the system in an off state until the power button is pressed again.

Power On

The Power On option restarts the system when the power has returned.

Last State

The Last State option restores the system to its previous state when the power was interrupted.

6.7.4.1.2. USB S4 WakeUp

The USB S4 WakeUp enables the system to resume through the USB device port from S4 state. There are two options: "Enabled" or "Disabled".

6.7.5. HDAC Configuration

HDAC Configuration Parameters.

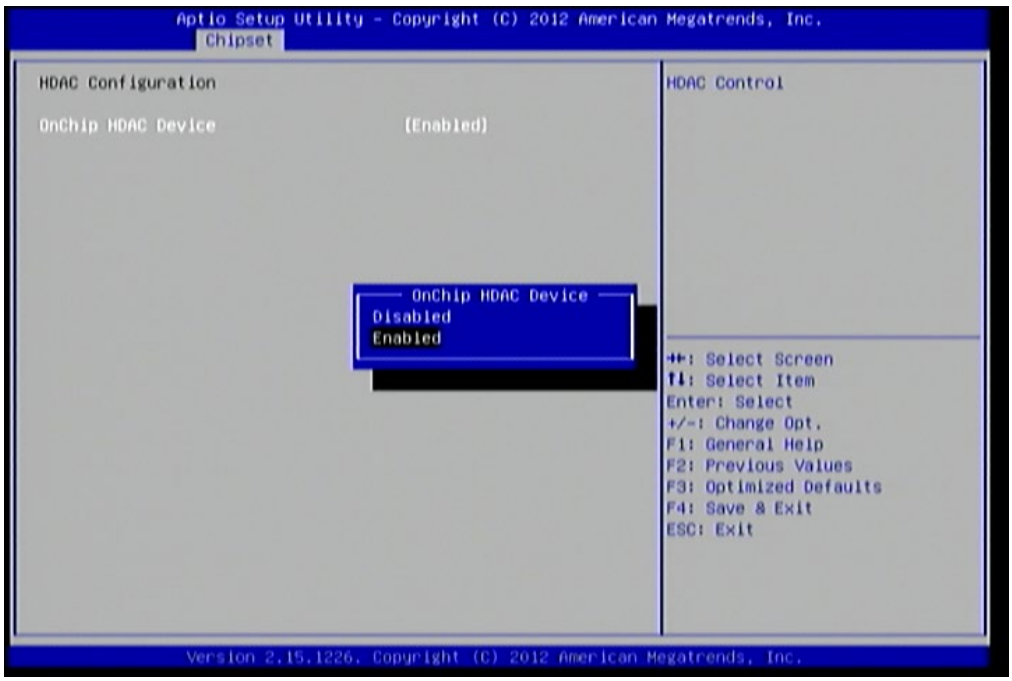

Figure 68: Illustration of HDAC Configuration screen

6.7.5.1. OnChip HDAC Device

This feature has 2 options: Enable or Disable HDAC Control.

6.7.6. SDIO_CR Configuration

The SDIO_CR Configuration screen can be used to set SDIO_CR configuration parameters.

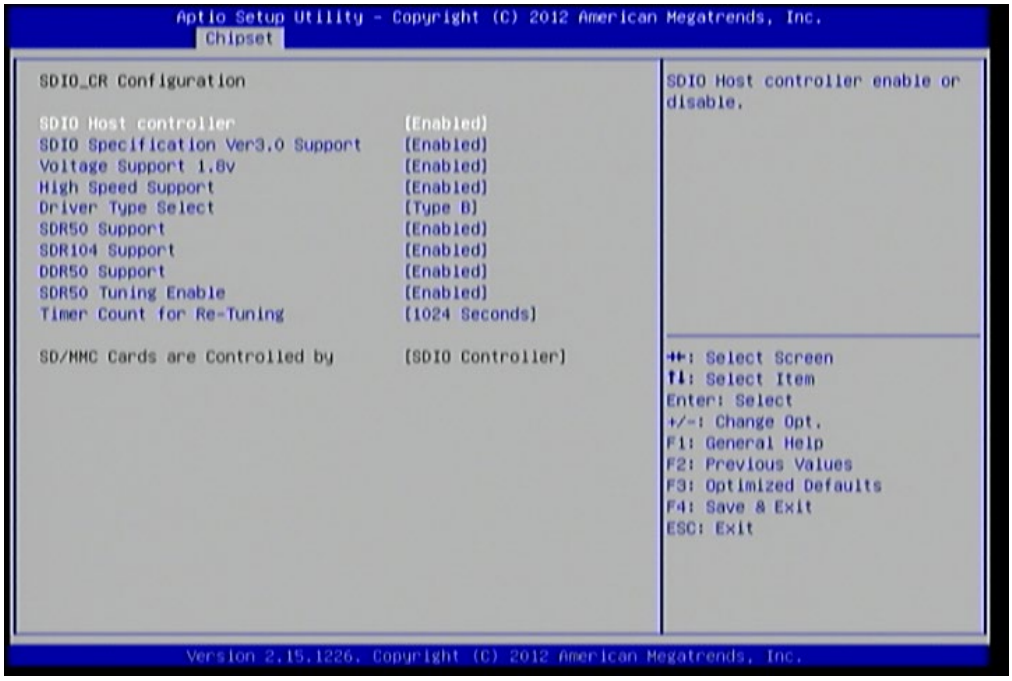

Figure 69: Illustration of SDIO_CR Configuration screen

6.7.6.1.1. SDIO Host Controller

This feature has two options: Enable or Disable SDIO Host controller.

6.7.6.1.2. SDIO Specification Ver3.0 Support

This feature has two options: Enable or Disable SDIO Specification Ver3.0 Support.

6.7.6.1.3. Voltage Support 1.8v

This feature has two options: Enable or Disable Voltage Support 1.8v.

6.7.6.1.4. High Speed Support

This feature has two options: Enable or Disable High Speed Support.

6.7.6.1.5. Driver Type Select

Select Driver Type from Type A Type B, Type C and Type D.

6.7.6.1.6. SDR50 Support

This feature has two options: Enable or Disable SDR50 Support.

6.7.6.1.7. SDR104 Support

This feature has two options: Enable or Disable SDR104 Support.

6.7.6.1.8. DDR50 Support

This feature has two options: Enable or Disable DDR50 Support.

6.7.6.1.9. SDR50 Tuning Enable

This feature has two options: Enable or Disable SDR50 Tuning Enable.

6.7.6.1.10. Timer Count for Re-Tuning

SDIO Timer Count for Re-Tuning. Available options are Re-Tuning Timer Disabled/1 sec/2 sec/4 sec/8 sec/16 sec/32 sec/64 sec/128 sec/256 sec/512 sec/1024 sec/Get information from other source.

6.7.7. Others Configuration

The Others Configuration screen can be used to set Watchdog Timer Configuration and Keyboard/Mouse Wakeup Configuration.

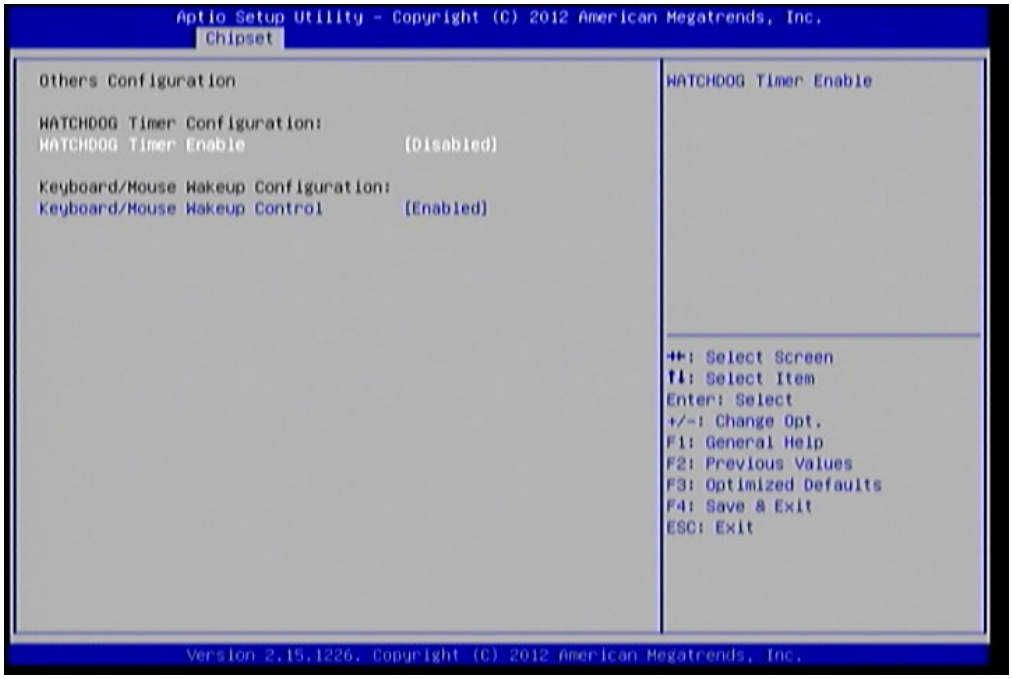

Figure 70: Illustration of Others Configuration screen

6.7.7.1. WATCHDOG Timer Enable

When this feature is enabled, an embedded timing device automatically prompts corrective action upon system malfunction detection.

6.7.7.2. Keyboard/Mouse Wakeup Control

When this feature is enabled, pressing any key of the keyboard or moving the mouse can wake up the system from suspend.

6.8. Boot Settings

The Boot Settings screen has a single link that goes to the **Boot Configuration,** and **Boot Option Priority** screens.

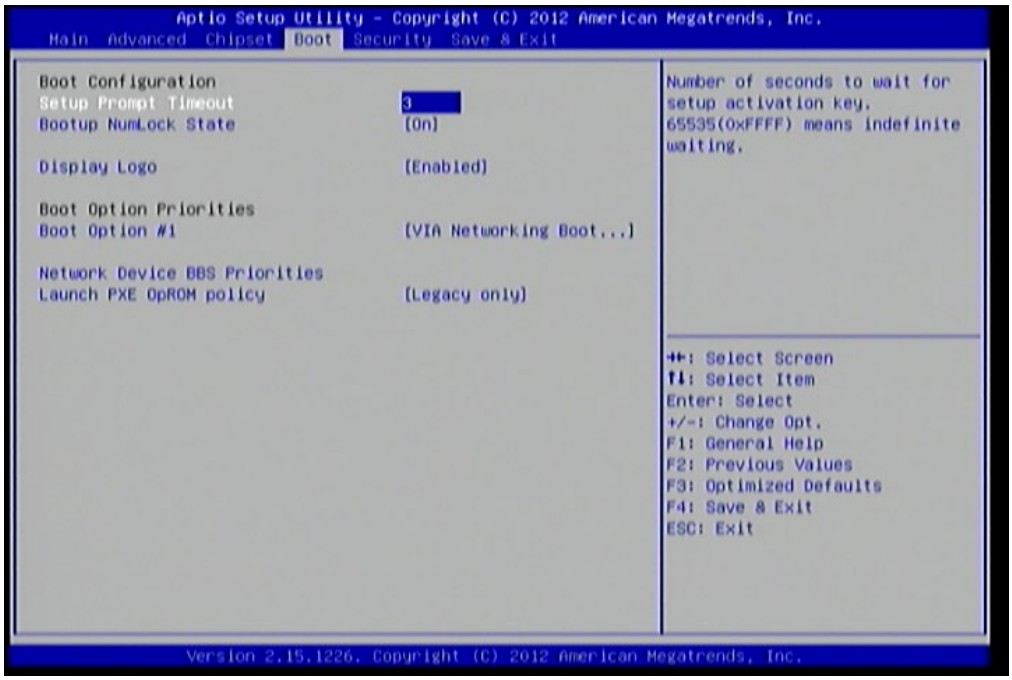

Figure 71: Illustration of Boot Settings screen

6.8.1. Boot Configuration

The Boot Settings Configuration screen has several features that can be run during the system boot sequence.

6.8.1.1. Setup Prompt Timeout

Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.

6.8.1.2. BootupNumLock State

Select the keyboard NumLock state from On and Off.

6.8.1.3. Display Logo

The Display Logo feature hides all of the Power-on Self Test (POST) messages during the boot sequence. Instead of the POST messages, the user will see an OEM logo. This feature has two options: enabled and disabled.

6.8.2. Boot Option Priorities

The Boot Option Priorities screen lists all bootable devices.

6.8.2.1. Boot Option #1

Sets the system boot order. This feature has two options: VIA Networking Bootagent/Disabled.

6.8.3. Network Device BBS Priorities

6.8.3.1. Launch PXE OpROM policy

Do not launch
Prevent the option for Legacy Network Device.

Legacy only
Allow the option for Legacy Network Device.

6.9. Security Settings

The Security Settings screen provides a way to restrict access to the BIOS or even the entire system.

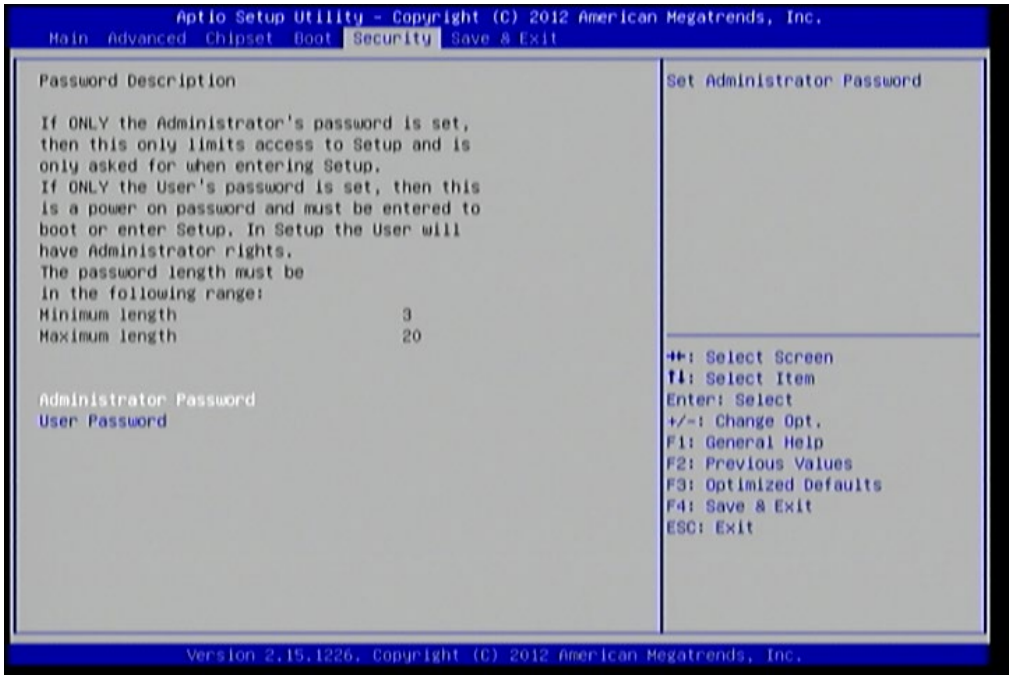

Figure 72: Illustration of Security Settings screen

6.9.1. Security Settings

6.9.1.1. Administrator Password / User Password

This option is for setting a password for accessing the BIOS setup utility. When a password has been set, a password prompt will be displayed whenever the BIOS setup utility is launched. This prevents an unauthorized person from changing any part of the system configuration.

When a supervisor password is set, the **Password Check** option will be unlocked.

6.9.1.2. Password Check

This feature is compulsory when the **Change Supervisor Password** option is set. The user will have up to three chances to enter the correct password before the BIOS forces the system to stop booting. If the user does not enter the correct password, the keyboard will also lock up. The only way to get past this is to do a hard reboot (i.e., use the system reset button or cut off the power to the system). A soft reboot (i.e., Ctrl+Alt+Del) will not work because the keyboard will be locked. This feature has two options.

Setup
The Setup option forces users to enter a password in order to access the BIOS Setup Utility.

Always
The Always option forces users to enter a password in order to boot up the system.

6.10. Save & Exit Options

The Save & Exit screen has the following features:

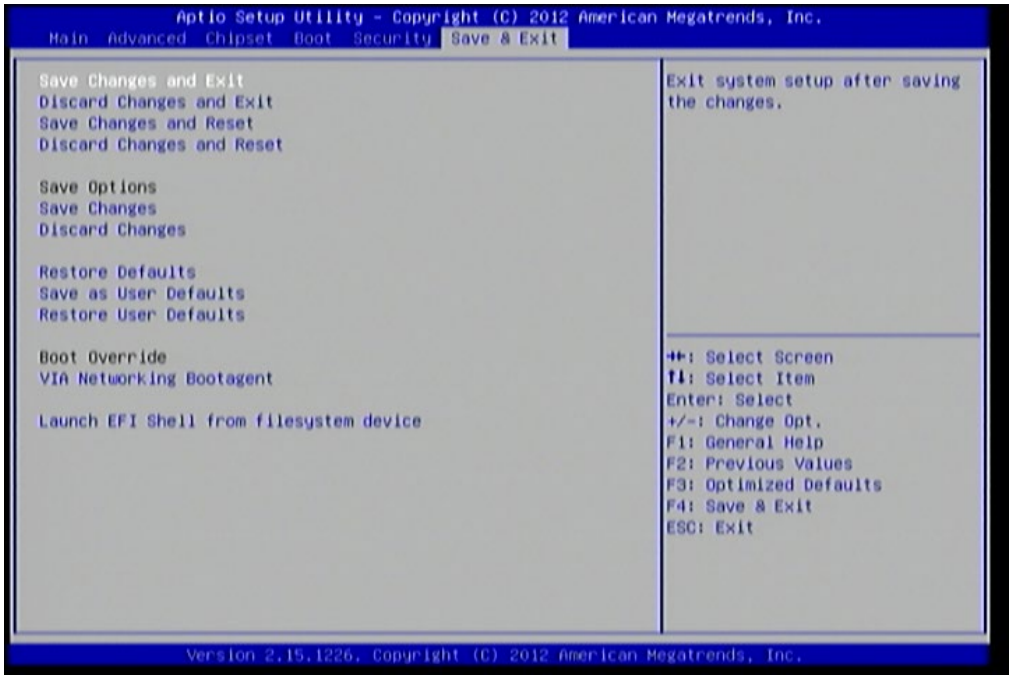

Figure 73: Illustration of Save & Exit Options screen

6.10.1. Save Changes and Exit

Save all changes to the BIOS and exit the BIOS Setup Utility. The "F4" hotkey can also be used to trigger this command.

6.10.2. Discard Changes and Exit

Exit the BIOS Setup Utility without saving any changes. The "Esc" hotkey can also be used to trigger this command.

6.10.3. Save Changes and Reset

Save all changes to the BIOS and reboot the system. The new system configuration parameters will take effect.

6.10.4. Discard Changes and Reset

This command reverts all changes to the settings that were in place when the BIOS Setup Utility was launched. The "F2" hotkey can also be used to trigger this command.

Save Options

6.10.5. Save Changes

Save Changes done so far to any of the setup options.

6.10.6. Discard Changes

This command reverts all changes to the settings that were in place when the BIOS Setup Utility was launched.

Boot Override

6.10.7. VIA Networking Bootagent

6.10.8. Launch EFI Shell from filesystem device

Attempts to Launch EFI Shell application (Shellx64.efi) from one of the available filesystem devices.

7. Software and Technical Support

7.1. Microsoft and Linux Support

The VIA EPIA-M920 is compatible with Microsoft Windows and Linux operating systems.

7.1.1. Driver Installation

Microsoft Driver Support

The latest windows drivers can be downloaded from the VIA website at www.viatech.com.

Linux Driver Support

Linux drivers are provided through various methods including:

- Drivers provided by VIA (binary only). An ARCM or NDA/BSLA may be asked in order to get the drivers, please contact our sales representative to submit a request.
- Using a driver built into a distribution package
- Installing a third party driver (such as the ALSA driver from the Advanced Linux Sound Architecture project for integrated audio)

7.2. Technical Support and Assistance

- For utilities downloads, latest documentation and information about the VIA EPIA-M920, please visit our website at http://www.viatech.com/en/boards/mini-itx/epia-m920
- For technical support and additional assistance, always contact your local sales representative or board distributor, or go to https://www.viatech.com/en/support/technical-support for technical support.
- For OEM clients and system integrators developing a product for long term production, other code and resources may also be made available. Please visit our website at https://www.viatech.com/en/about/contact to submit a request.

Appendix A. Installing Wireless Accessories

This chapter provides you with information on how to install the VIA EMIO wireless module into the VIA EPIA-M920. It is recommended to use a grounded wrist strap before handling computer components. Electrostatic discharge (ESD) can damage some components.

A.1. Installing the VIA EMIO-1533 USB Wi-Fi Module

Step 1

Mount the VIA EMIO-1533 module to the prepared standoff in the chassis. Align the two mounting holes on the VIA EMIO-1533 module with the mounting holes on the standoffs, and then secure the VIA EMIO-1533 module in place with two screws.

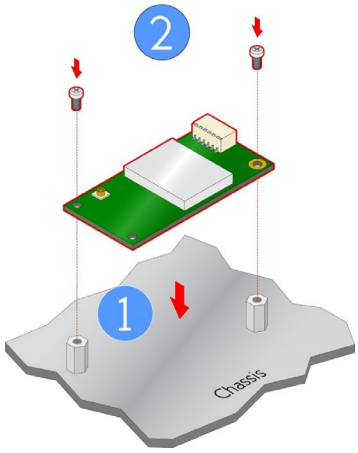

Figure 74: Installing VIA EMIO-1533 module to the chassis

Step 2

Connect one end of the USB Wi-Fi cable to the onboard USB 2.0 connector (USB_1) on VIA EPIA-M920 board, and then connect the other end of the cable to the VIA EMIO-1533 module.

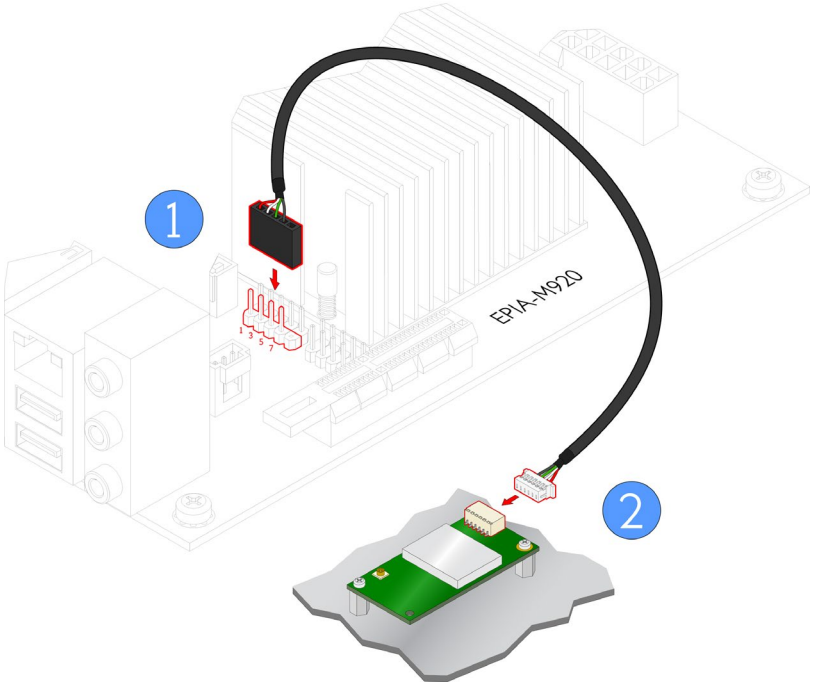

Figure 75: Connecting the USB Wi-Fi cable (VIA EMIO-1533)

Step 3

Insert the Wi-Fi antenna cable into the antenna hole from the inside of the panel I/O plate. Insert the toothed washer, fasten it with the nut, and install the external antenna.

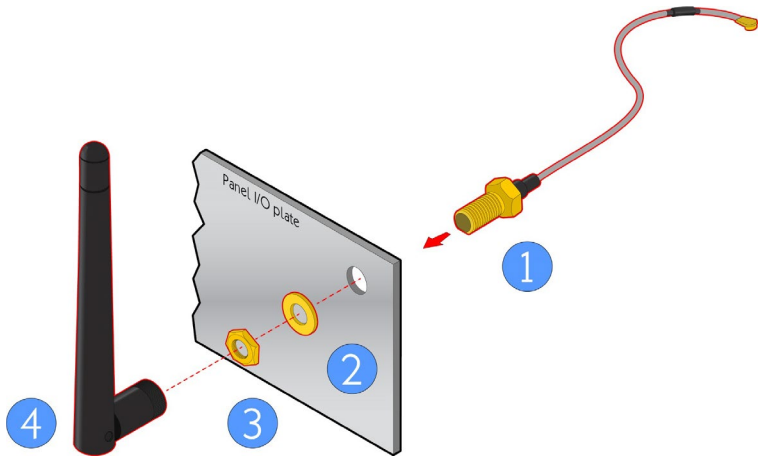

Figure 76: Installing Wi-Fi antenna cable (VIA EMIO-1533)

Step 4

Connect the other end of the Wi-Fi antenna cable to the micro-RF connector labeled "I-PEX" on the VIA EMIO-1533 module.

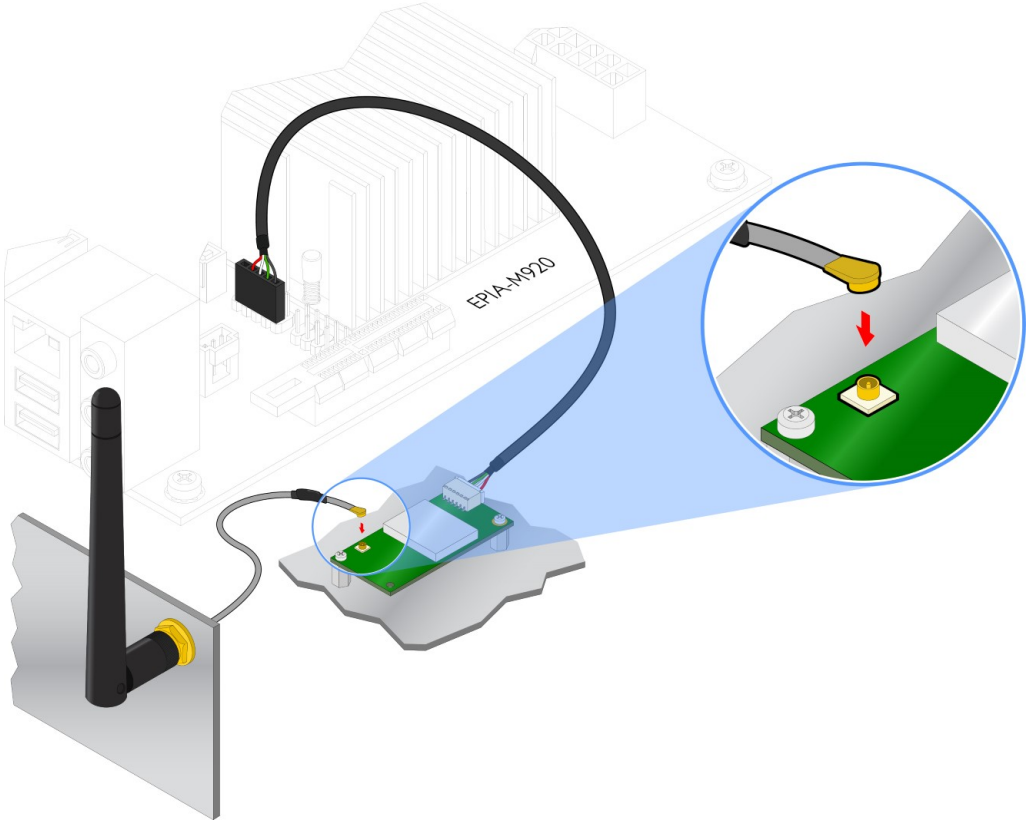

Figure 77: Connecting Wi-Fi antenna cable to the micro-RF connector (VIA EMIO-1533)

A.2. Installing the VIA EMIO-5531 USB Wi-Fi & Bluetooth Module

Step 1

Mount the VIA EMIO-5531 module to the prepared standoff in the chassis. Align the two mounting holes on the VIA EMIO-5531 module with the mounting holes on the standoffs, and then secure the VIA EMIO-5531 module in place with two screws.

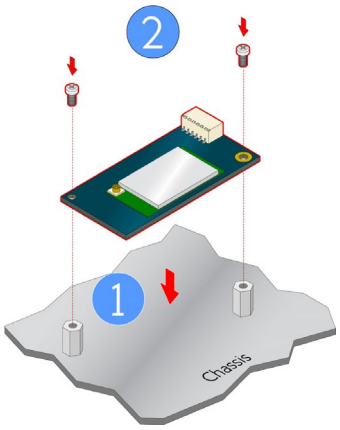

Figure 78: Installing VIA EMIO-5531 module to the chassis

Step 2

Connect one end of the USB Wi-Fi cable to the onboard USB 2.0 connector (USB_1) on the VIA EPIA-M920 board, and then connect the other end of the cable to the VIA EMIO-5531 module.

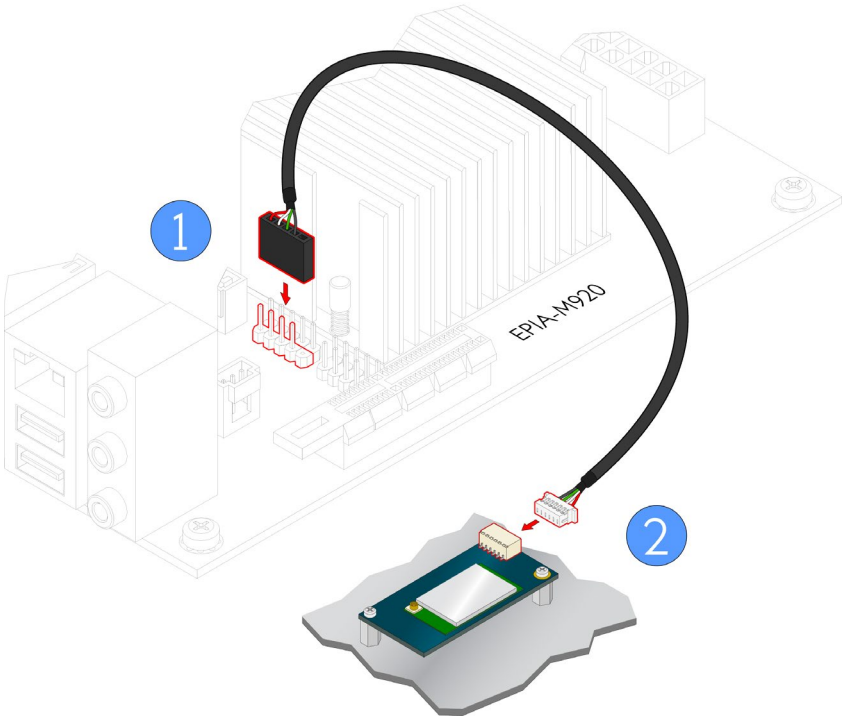

Figure 79: Connecting the USB Wi-Fi cable (VIA EMIO-5531)

Step 3

Insert the Wi-Fi antenna cable into the antenna hole from the inside of the panel I/O plate. Insert the toothed washer, fasten it with the nut, and install the external antenna.

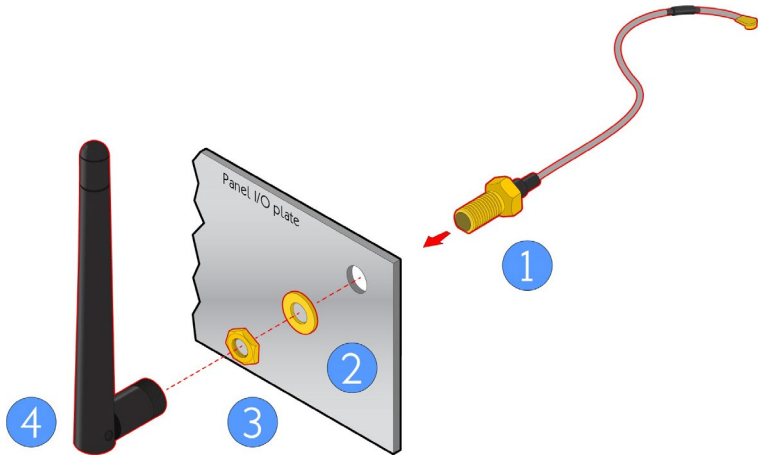

Figure 80: Installing Wi-Fi antenna cable (VIA EMIO-5531)

Step 4

Connect the other end of the Wi-Fi antenna cable to the micro-RF connector labeled "I-PEX" on the VIA EMIO-5531 module.

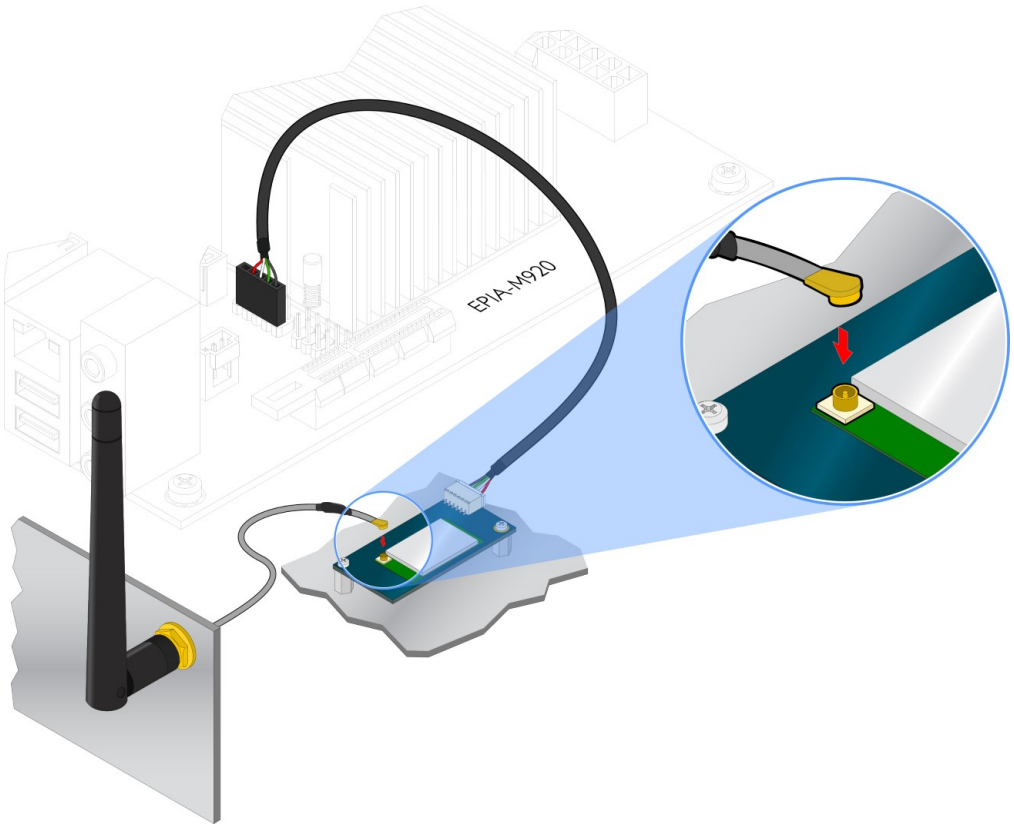

Figure 81: Connecting Wi-Fi antenna cable to the micro-RF connector (VIA EMIO-5531)

Appendix B. Power Consumption Report

Power consumption tests were performed on the VIA EPIA-M920. The following tables represent the breakdown of the voltage, amp and wattage values while running common system applications.

B.1. VIA EPIA-M920 Rev. B ATX Power (EPIA-M920-20Q SKU)

The tests were performed based on the following additional components:

- **CPU:** 2.0GHz VIA QuadCore E-Series
- **Memory:** Kingston DDR3 1333MHz 4GB
- **HDD:** SATAII 2TB WD WD20EARX
- **System OS:** Windows 7 64-bit
- **ATX PSU:** CWT CWT-430AS 410W

B.1.1. IDLE Status

MEAN	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.087	0.130	0.401
Main Board +5V	4.777	0.668	3.191
Main Board 5VSB	4.646	0.546	2.537
Main Board +12V	11.767	0.590	6.943
Main Board Power Consumption			13.072

MAX	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.097	0.155	0.480
Main Board +5V	4.790	0.714	3.420
Main Board 5VSB	4.692	0.671	3.148
Main Board +12V	11.778	0.641	7.550
Main Board Power Consumption			14.598

B.1.2. S3 Status

MEAN	Measured Voltage	Measured Current	Watts
Main Board +3.3V	0.004	0.000	0.000
Main Board +5V	0.015	0.000	0.000
Main Board 5VSB	5.096	0.147	0.749
Main Board +12V	0.000	0.000	0.000
Main Board Power Consumption			0.749

MAX	Measured Voltage	Measured Current	Watts
Main Board +3.3V	0.013	0.000	0.000
Main Board +5V	0.019	0.000	0.000
Main Board 5VSB	5.099	0.173	0.882
Main Board +12V	0.000	0.000	0.000
Main Board Power Consumption			0.882

B.1.3. MP3 Playing (Windows Media Player 10)

MEAN	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.217	0.547	1.760
Main Board +5V	4.954	0.964	4.776
Main Board 5VSB	5.005	0.328	1.642
Main Board +12V	11.901	0.689	8.200
Main Board Power Consumption			16.377

MAX	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.228	0.585	1.888
Main Board +5V	4.964	0.862	4.279
Main Board 5VSB	5.017	0.364	1.826
Main Board +12V	11.909	0.918	10.932
Main Board Power Consumption			18.926

B.1.4. MP4 Playing (Windows Media Player 10)

MEAN	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.117	0.487	1.518
Main Board +5V	4.832	1.081	5.223
Main Board 5VSB	4.887	0.474	2.316
Main Board +12V	11.794	0.732	8.633
Main Board Power Consumption			17.691

MAX	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.211	0.520	1.670
Main Board +5V	4.942	1.377	6.805
Main Board 5VSB	4.992	0.745	3.719
Main Board +12V	11.897	0.916	10.898
Main Board Power Consumption			23.092

B.1.5. Graphics: Run 3D Marks'06

MEAN	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.050	0.498	1.519
Main Board +5V	4.666	1.202	5.609
Main Board 5VSB	4.424	0.768	3.398
Main Board +12V	11.710	0.714	8.361
Main Board Power Consumption			18.886

MAX	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.110	0.552	1.717
Main Board +5V	4.811	2.095	10.079
Main Board 5VSB	4.722	0.984	4.646
Main Board +12V	11.811	1.313	15.508
Main Board Power Consumption			31.950

B.1.6. Functional Test: Run BurnIn Test 6.0

MEAN	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.043	0.462	1.406
Main Board +5V	4.635	1.228	5.692
Main Board 5VSB	4.511	0.856	3.861
Main Board +12V	11.663	1.005	11.721
Main Board Power Consumption			22.680

MAX	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.088	0.511	1.578
Main Board +5V	4.796	1.649	7.909
Main Board 5VSB	4.717	1.005	4.741
Main Board +12V	11.781	1.263	14.879
Main Board Power Consumption			29.107

B.1.7. GigaLAN Network Access x2 Ports

MEAN	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.112	0.596	1.855
Main Board +5V	4.688	1.150	5.391
Main Board 5VSB	4.653	0.608	2.829
Main Board +12V	11.698	0.746	8.727
Main Board Power Consumption			18.802

MAX	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.147	0.629	1.979
Main Board +5V	4.715	1.489	7.021
Main Board 5VSB	4.712	0.732	3.449
Main Board +12V	11.788	0.883	10.409
Main Board Power Consumption			22.858

B.1.8. S5 Status

MEAN	Measured Voltage	Measured Current	Watts
Main Board +3.3V	0.008	0.000	0.000
Main Board +5V	0.020	0.000	0.000
Main Board 5VSB	5.105	0.098	0.500
Main Board +12V	0.000	0.000	0.000
Main Board Power Consumption			0.500

MAX	Measured Voltage	Measured Current	Watts
Main Board +3.3V	0.025	0.000	0.000
Main Board +5V	0.038	0.000	0.000
Main Board 5VSB	5.109	0.123	0.628
Main Board +12V	0.000	0.000	0.000
Main Board Power Consumption			0.628

B.2. VIA EPIA-M920 Rev. B ATX Power (EPIA-M920-16QE SKU)

The tests were performed based on the following additional components:

- **CPU:** 1.6GHz VIA Eden® X4
- **Memory:** Kingston DDR3 1333MHz 4GB
- **HDD:** SATAII 2TB WD WD20EARX
- **System OS:** Windows 7 64-bit
- **ATX PSU:** CWT CWT-430AS 410W

B.2.1. IDLE Status

MEAN	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.264	0.351	1.146
Main Board +5V	5.010	0.752	3.768
Main Board 5VSB	5.063	0.333	1.686
Main Board +12V	11.959	0.386	4.616
Main Board Power Consumption			11.215

MAX	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.275	0.431	1.412
Main Board +5V	5.020	1.036	5.201
Main Board 5VSB	5.074	0.367	1.862
Main Board +12V	11.970	0.503	6.021
Main Board Power Consumption			14.495

B.2.2. S3 Status

MEAN	Measured Voltage	Measured Current	Watts
Main Board +3.3V	0.014	0.000	0.000
Main Board +5V	0.000	0.000	0.000
Main Board 5VSB	5.111	0.144	0.736
Main Board +12V	0.000	0.000	0.000
Main Board Power Consumption			0.736

MAX	Measured Voltage	Measured Current	Watts
Main Board +3.3V	0.025	0.000	0.000
Main Board +5V	0.030	0.000	0.000
Main Board 5VSB	5.115	0.172	0.880
Main Board +12V	0.000	0.000	0.000
Main Board Power Consumption			0.880

B.2.3. MP3 Playing (Windows Media Player 10)

MEAN	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.150	0.467	1.471
Main Board +5V	4.899	0.704	3.449
Main Board 5VSB	4.954	0.374	1.853
Main Board +12V	11.852	0.437	5.179
Main Board Power Consumption			11.952

MAX	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.158	0.514	1.623
Main Board +5V	4.907	0.929	4.559
Main Board 5VSB	4.964	0.452	2.244
Main Board +12V	11.859	0.455	5.396
Main Board Power Consumption			13.821

B.2.4. MP4 Playing (Windows Media Player 10)

MEAN	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.059	0.471	1.441
Main Board +5V	4.721	1.243	5.868
Main Board 5VSB	4.764	0.841	4.007
Main Board +12V	11.696	0.447	5.228
Main Board Power Consumption			16.544

MAX	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.120	0.509	1.588
Main Board +5V	4.846	1.638	7.938
Main Board 5VSB	4.896	0.987	4.832
Main Board +12V	11.808	0.553	6.530
Main Board Power Consumption			20.888

B.2.5. Graphics: Run 3D Marks'06

MEAN	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.060	0.487	1.490
Main Board +5V	4.698	1.293	6.075
Main Board 5VSB	4.749	0.806	3.828
Main Board +12V	11.679	0.408	4.765
Main Board Power Consumption			16.157

MAX	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.100	0.516	1.600
Main Board +5V	4.820	2.287	11.023
Main Board 5VSB	4.870	0.917	4.466
Main Board +12V	11.792	0.666	7.853
Main Board Power Consumption			24.942

B.2.6. Functional Test: Run BurnIn Test 6.0

MEAN	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.195	0.453	1.447
Main Board +5V	4.919	1.405	6.911
Main Board 5VSB	4.989	0.604	3.013
Main Board +12V	11.888	0.667	7.929
Main Board Power Consumption			19.301

MAX	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.250	0.491	1.596
Main Board +5V	4.986	1.850	9.224
Main Board 5VSB	5.043	0.725	3.656
Main Board +12V	11.940	0.814	9.719
Main Board Power Consumption			24.195

B.2.7. GigaLAN Network Access x2 Ports

MEAN	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.193	0.766	2.446
Main Board +5V	4.776	1.195	5.707
Main Board 5VSB	4.843	0.466	2.257
Main Board +12V	11.783	0.636	7.494
Main Board Power Consumption			17.904

MAX	Measured Voltage	Measured Current	Watts
Main Board +3.3V	3.231	0.778	2.514
Main Board +5V	4.803	1.431	6.873
Main Board 5VSB	4.872	0.485	2.363
Main Board +12V	11.818	0.713	8.426
Main Board Power Consumption			20.176

B.2.8. S5 Status

MEAN	Measured Voltage	Measured Current	Watts
Main Board +3.3V	0.006	0.000	0.000
Main Board +5V	0.018	0.000	0.000
Main Board 5VSB	5.105	0.085	0.434
Main Board +12V	0.000	0.000	0.000
Main Board Power Consumption			0.434

MAX	Measured Voltage	Measured Current	Watts
Main Board +3.3V	0.051	0.000	0.000
Main Board +5V	0.134	0.000	0.000
Main Board 5VSB	5.108	0.051	0.261
Main Board +12V	0.002	0.000	0.000
Main Board Power Consumption			0.261

Appendix C. Mating Connector Vendors List

The following table listed the mating connector vendors list of VIA EPIA-M920.

Connectors	Part No.	Mating Vendor & P/N	
Front panel pin header (F_PANEL)	99G30-05009I	Neltron 2214S-XXG-85	SAMTEC SSW Series
		Neltron 2214R-XXG-85	
Front audio pin header (F_AUDIO1)	99G30-05458I	Neltron 2207S-XXG	N.A.
		Neltron 2207R-XXG	
		Neltron 2207SM-XXG-45	
System fan connector (SYSFAN)	99G30-020035	Neltron 2218H-03	N.A.
Backlight control connectors (INVERTER1 & INVERTER2)	99G30-020537	ACES 85206-0800	MOLEX 51021-**00
LVDS panel connectors (LVDS1 & LVDS2)	99G30-170152	ACES 44002-XX00	DF13-**DS-1.258C
USB 2.0 pin header (USB_1 & USB_2)	99G30-05072K	Neltron 2214S-XXG-85	SAMTEC SSW Series
		Neltron 2214R-XXG-85	

Table 38: VIA EPIA-M920 mating connector vendors list

Taiwan Headquarters

1F, 531 Zhong-zheng Road,
Xindian Dist., New Taipei City 231
Taiwan

Tel: 886-2-2218-5452
Fax: 886-2-2218-9860
Email: embedded@via.com.tw

USA

940 Mission Court
Fremont, CA 94539,
USA

Tel: 1-510-687-4688
Fax: 1-510-687-4654
Email: embedded@viatech.com

Japan

3-15-7 Ebisu MT Bldg. 6F,
Higashi, Shibuya-ku
Tokyo 150-0011
Japan

Tel: 81-3-5466-1637
Fax: 81-3-5466-1638
Email: embedded@viatech.co.jp

China

Tsinghua Science Park Bldg. 7
No. 1 Zongguancun East Road,
Haidian Dist., Beijing, 100084
China

Tel: 86-10-59852288
Fax: 86-10-59852299
Email: embedded@viatech.com.cn

Europe

Email: embedded@via-tech.eu