USER MANUAL

VIA EPIA-P910

Highly-integrated low-power platform with rich multimedia and I/O capabilities

2.05-07022020-154800

Copyright

Trademarks

All trademarks are the property of their respective holders.

Disclaimer

No license is granted, implied or otherwise, under any patent or patent rights of VIA Technologies. VIA Technologies makes no warranties, implied or otherwise, in regard to this document and to the products described in this document. The information provided in this document is believed to be accurate and reliable as of the publication date of this document. However, VIA Technologies assumes no responsibility for the use or misuse of the information (including use or connection of extra device/equipment/add-on card) in this document and for any patent infringements that may arise from the use of this document. The information and product specifications within this document are subject to change at any time, without notice and without obligation to notify any person of such change.

VIA Technologies, Inc. reserves the right the make changes to the products described in this manual at any time without prior notice.

Regulatory Compliance

FCC-A Radio Frequency Interference Statement

This equipment has been tested and found to comply with the limits for a class A digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his personal expense.

Notice 1

The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Notice 2

Shielded interface cables and A.C. power cord, if any, must be used in order to comply with the emission limits.

Notice 3

The product described in this document is designed for general use, VIA Technologies assumes no responsibility for the conflicts or damages arising from incompatibility of the product. Check compatibility issue with your local sales representatives before placing an order.

CE

FC Tested To Comply
With FCC Standards
FOR HOME OR OFFICE USE

Battery Recycling and Disposal

- ☐ Only use the appropriate battery specified for this product.
- ☐ Do not re-use, recharge, or reheat an old battery.
- ☐ Do not attempt to force open the battery.
- ☐ Do not discard used batteries with regular trash.
- ☐ Discard used batteries according to local regulations.

Safety Precautions

- ☐ Always read the safety instructions carefully.
- ☐ Keep this User's Manual for future reference.
- ☐ All cautions and warnings on the equipment should be noted.
- ☐ Keep this equipment away from humidity.
- ☐ Put this equipment on a reliable flat surface before setting it up.
- ☐ Check the voltage of the power source and adjust properly 110/220V before connecting the equipment to the power inlet.
- ☐ Do not place the power cord where people will step on it.
- ☐ Always unplug the power cord before inserting any add-on card or module.
- ☐ If any of the following situations arise, get the equipment checked by authorized service personnel:
  - The power cord or plug is damaged.
  - Liquid has entered into the equipment.
  - The equipment has been exposed to moisture.
  - The equipment is faulty or you cannot get it work according to User's Manual.
  - The equipment has been dropped and damaged.
  - The equipment has an obvious sign of breakage.
- ☐ Do not leave this equipment in extreme temperatures or in a storage temperature above 60°C (140°F). The equipment may be damaged.
- ☐ Do not leave this equipment in direct sunlight.
- ☐ Never pour any liquid into the opening. Liquid can cause damage or electrical shock.
- ☐ Do not place anything over the power cord.
- ☐ Do not cover the ventilation holes. The openings on the enclosure protect the equipment from overheating.

Box Contents

- ☐ 1 x VIA EPIA-P910 board
- ☐ 1 x SATA cable
- ☐ 1 x SATA power cable
- ☐ 1 x DC power cable

Ordering Information

Model Name	Description
EPIA-P910-12QE	Pico-ITX board with 1.2GHz VIA Eden® X4 CPU, Mini HDMI, VGA, LVDS, 2 x USB 3.0, 6 x USB 2.0, Gigabit Ethernet, 2 x SATA and 12V DC-in

Optional Accessories

I/O Expansion Cards

Part Number	Description
EPIA-P910-A	Front I/O card with 2 LEDs, 1 power button, 3 audio jacks and 2 USB 2.0

Wireless Modules

Part Number	Description
EMIO-1533-00A2	VNT9271 IEEE 802.11b/g/n USB Wi-Fi module with assembly kit and antenna
EMIO-5531-00A1	VAB-820-W IEEE 802.11b/g/n USB Wi-Fi & Bluetooth module with assembly kit and antenna

Table of Contents

List of Figures

List of Tables

1. Product Overview

The VIA EPIA-P910 integrates the advanced performance of the 1.2GHz VIA Eden® X4 processor with the superior multimedia capabilities of the VIA VX11H media system processor on a highly compact Pico-ITX form factor to provide a versatile platform for building a diverse range of ultra-small form factor devices for healthcare, logistics, fleet management and a myriad of other vertical market applications

Based on the Pico-ITX form factor measuring just 10cm x 7.2cm, the VIA EPIA-P910 comes with a rich set of I/O and connectivity features, including two USB 3.0 ports, one Gigabit Ethernet port, one Mini HDMI port, and one VGA port. The functionality of the VIA EPIA-P910 can be enhanced using its onboard pin headers and a variety of expansion cards and modules.

The VIA EPIA-P910 includes one 1333MHz DDR3 SODIMM slot that support up to 8GB memory size, and provides support for high fidelity audio with its included VIA VT2021 High Definition Audio codec. In addition, it supports two SATA 3.0Gbps storage devices and fully compatible with Microsoft Windows and Linux operating systems.

1.1. Key Features and Benefits

1.1.1. VIA Eden® X4 Processor

The VIA Eden® X4 is a 64-bit superscalar x86 multi-core processor combine on two dies. It is based on advanced 28 nanometer process technology packed into an ultra-compact NanoBGA2 package measuring 21mm x 21mm. The VIA Eden® X4 processor delivers a superb performance on multi-tasking, multimedia playback, productivity and internet browsing in a low power budget. In addition, it is ideal for most of multi-display environment, and embedded system applications such as industrial PCs, test machines, measuring equipment, digital signage, medical PCs, monitoring systems, gaming machines, in-vehicle entertainment, etc.

1.1.2. VIA VX11H MSP Chipset

The VIA VX11H is the fourth generation, highly integrated Media System Processor which provides high quality digital video streaming and high definition video playback. It features the VIA C-640 DX11 3D/2D graphics and video processor, High Definition video decoder supports DDR3 1333 controller and USB 3.0 interface.

The VIA VX11H offers superb-graphics performance, immersive visual experience, and supports DirectX 11.0 that allows realistic 3D rendering and increased visual acuity. The VIA VX11H is based on a highly sophisticated power efficient architecture that enables such rich integration into a compact package.

1.1.3. Expansion Option

The VIA EPIA-P910 further proves its versatility by providing an optional expansion connector. The VIA EPIA-P910-A I/O expansion card is connected through onboard pin headers carrying the front panel I/O such as audio jack, USB 2.0 ports, LED indicator and power button.

The companies using the VIA EPIA-P910 with VIA EPIA-P910-A I/O expansion card obtain the maximum benefits and enable to slowly roll out upgrades as necessary instead of having to replace everything all at once.

1.2. Product Specifications

- **Processor**
  - 1.2GHz VIA Eden® X4 (Fanless)

- **Chipset**
  - VIA VX11H MSP

- **Graphics**
  - Integrated VIA C-640 DX11 3D/2D graphics and video processor
  - MPEG-2, WMV9, VC-1, and H.264 Full HD video decoder
  - UMA supporting CRT/HDMI/LVDS
  - Optimized Unified Memory Architecture (UMA)
  - Support frame buffer size from 256MB to 512MB

- **System Memory**
  - 1 x SODIMM slot supporting DDR3 1333MHz
  - Supports up to 8GB memory size

- **Onboard Peripherals**
  - **Serial ATA**
    - Supports up to two SATA 3Gbps
  - **Onboard LAN**
    - VIA VT6130 PCIe Gigabit Ethernet controller
  - **Onboard Audio**
    - VIA VT2021 High Definition Audio Codec
  - **Onboard Super I/O**
    - Fintek F81801U-I Super I/O controller

- **Expansion I/O**
  - 3 x PCIe x1 and 3 x USB 2.0 (through High Speed Extension slot)

- **Onboard I/O**
  - 1 x KB/MS, LPC, SMBus and GPIO combination pin header
  - 1 x Front panel, Audio (Line-in / Line-out / Mic-in / S/PDIF-out), USB 2.0 combination pin header
  - 1 x Single-channel 18/24-bit LVDS panel connector
  - 2 x SATA connectors
  - 1 x SATA power connector (with Y-cable for 2)
  - 1 x System/CPU fan connector
  - 1 x LVDS panel power jumper (5V/3.3V)
  - 1 x Backlight power jumper (5V/12V)
  - 1 x SPI flash connector
  - 1 x CMOS external battery connector
  - 1 x DC-in connector

- **Back Panel I/O**
  - 1 x Mini HDMI® port (Type C)
  - 1 x VGA port
  - 1 x Gigabit Ethernet port
  - 2 x USB 3.0 ports

- **BIOS**
  - AMI Aptio UEFI BIOS
  - 32 Mbit SPI Flash memory

- **Supported Operating System**
  - Windows 10
  - Windows 8.1
  - Windows 8
  - Windows 7
  - Windows Embedded Standard 7
  - Linux

- **System Monitoring & Management**
  - Wake-on-LAN
  - Keyboard-Power-on
  - Timer-Power-on
  - System Power Management
  - AC power failure recovery
  - Watchdog Timer

- **Operating Temperature**
  - 0°C ~ 60°C

- **Operating Humidity**
  - 0% ~ 95% (non-condensing)

- **Form Factor**
  - Pico-ITX (10cm x 7.2cm, 3.9" x 2.8")

- **Compliance**
  - CE
  - FCC

Note:

As the operating temperature provided in the specifications is a result of testing performed in a testing chamber, a number of variables can influence this result. Please note that the working temperature may vary depending on the actual situation and environment. It is highly recommended to execute a solid testing program and take all variables into consideration when building the system. Please ensure that the system is stable at the required operating temperature in terms of application.

1.3. Layout Diagram

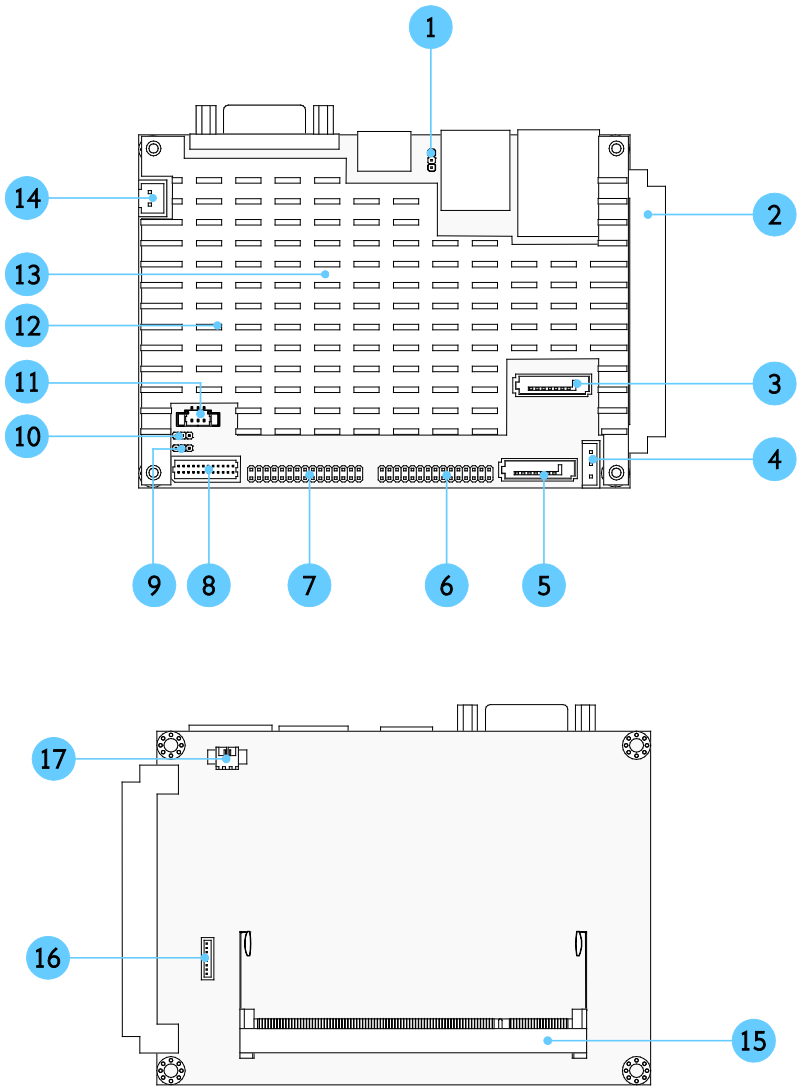

Figure 1: Layout diagram of the VIA EPIA-P910 (top and bottom side)

Item	Description
1	JM1: Clear CMOS jumper
2	CN3: High Speed Extension slot
3	SATA2: SATA connector 2
4	PWR2: SATA power connector
5	SATA1: SATA connector 1
6	CN2: Audio+USB 2.0+Front Panel combination pin header
7	CN1: KB/MS/LPC/GPIO/SMBus combination pin header
8	LVDS1: LVDS panel connector
9	JM3: LVDS panel power jumper
10	JM2: Backlight power jumper
11	FAN1: System/CPU fan connector
12	CPU: VIA Eden® X4
13	VX11H chipset
14	PWR1: DC-in power connector
15	SODIMM1: DDR3 SODIMM slot
16	J1: SPI flash connector
17	BAT1: CMOS battery connector

Table 1: Layout description table of the VIA EPIA-P910

1.4. Product Dimensions

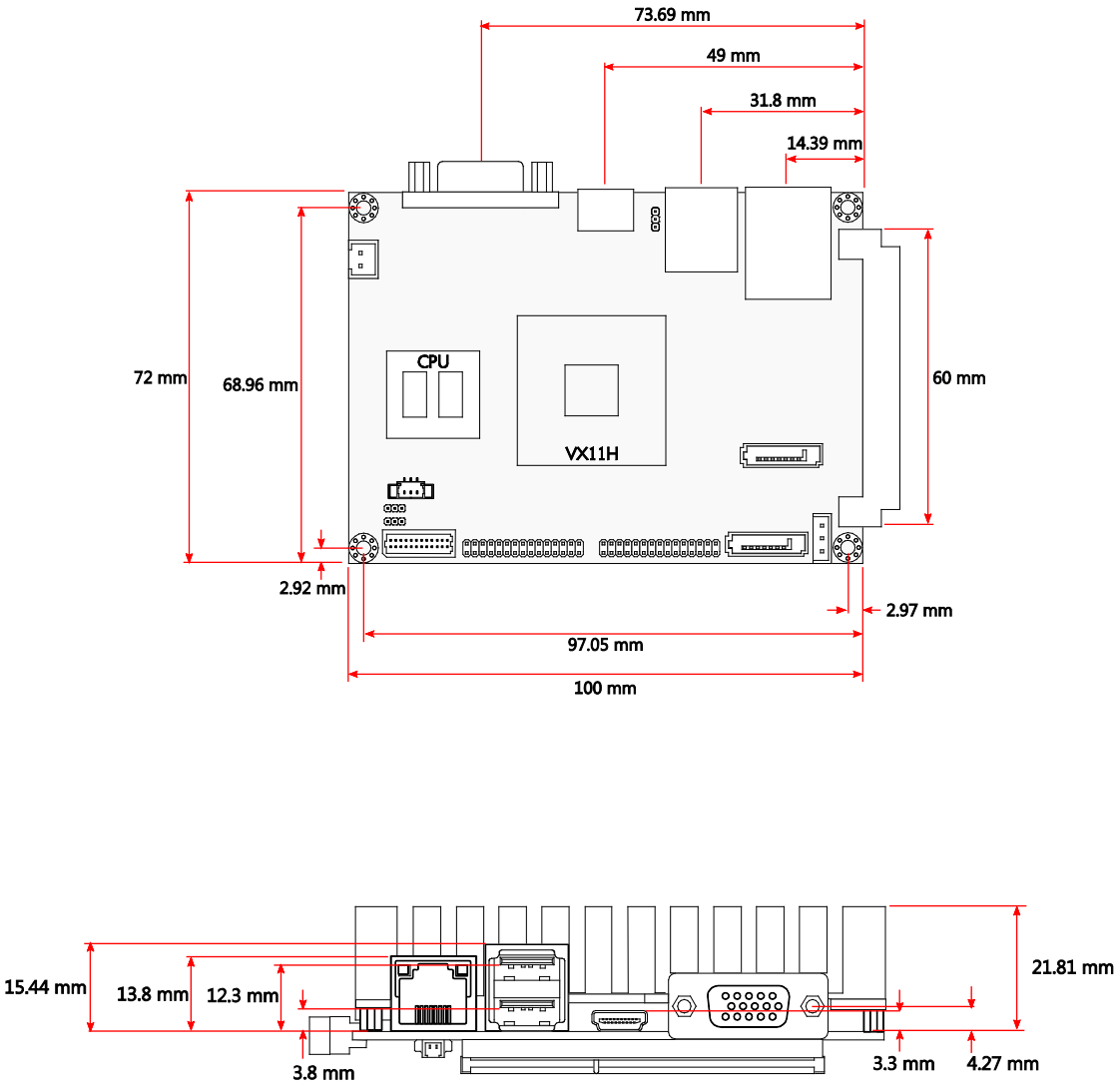

Figure 2: Mounting holes and dimensions of the VIA EPIA-P910

1.5. Height Distribution

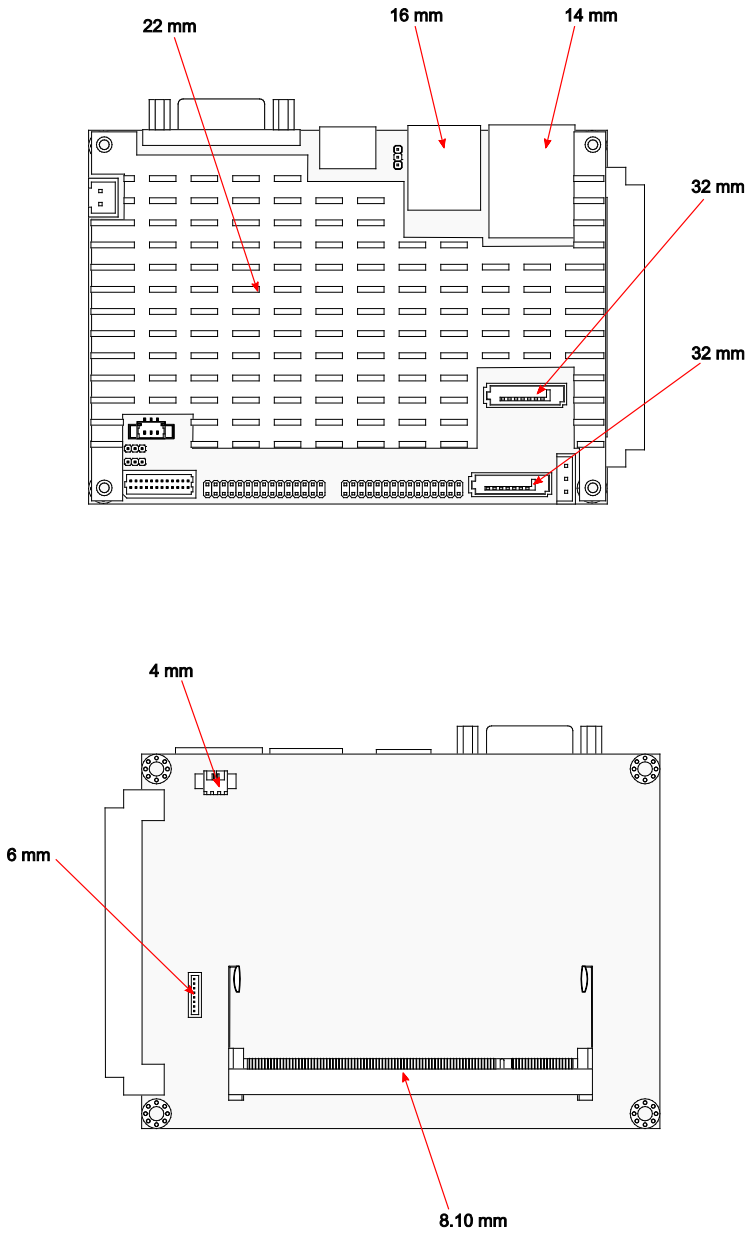

Figure 3: Height distribution of the VIA EPIA-P910

2. I/O Interface

The VIA EPIA-P910 has a wide selection of interfaces. It includes a selection of frequently used ports as part of the external I/O coastline.

2.1. External I/O Ports

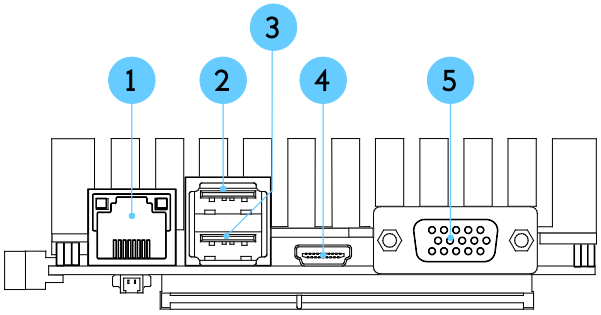

Figure 4: Back panel I/O ports

Item	Description
1	RJ1: Gigabit Ethernet port
2	USB1: USB 3.0 port
3	USB2: USB 3.0 port
4	HDMI1: Mini HDMI® port
5	VGA1: VGA port

Table 2: Layout description table of the back panel I/O ports

2.1.1. Gigabit Ethernet Port

The integrated 8-pin Gigabit Ethernet port is using an 8 Position 8 Contact (8P8C) receptacle connector commonly known as RJ-45. The Gigabit Ethernet port is controlled by VIA VT6130 PCIe Gigabit Ethernet controller. The pinouts of the Gigabit Ethernet port are shown below.

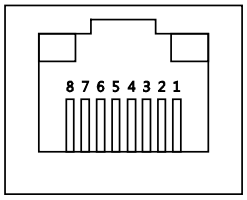

Figure 5: Gigabit Ethernet port diagram

Pin	Signal
1	Signal pair 1+
2	Signal pair 1-
3	Signal pair 2+
4	Signal pair 3+
5	Signal pair 3-
6	Signal pair 2-
7	Signal pair 4+
8	Signal pair 4-

Table 3: Gigabit Ethernet port pinouts

The Gigabit Ethernet port has two individual LED indicators located on the front side to show its Active/Link status and Speed status.

	Link LED (Left LED on RJ-45 connector)	Active LED (Right LED on RJ-45 connector)
Link Off	Off	Off
Speed_10Mbit	The LED is always On in either Green or Orange colors	Flash in Yellow color
Speed_100Mbit	The LED is always On in Green color	Flash in Yellow color
Speed_1000Mbit	The LED is always On in Orange color	Flash in Yellow color

Table 4: Gigabit Ethernet LED color definition

2.1.2. USB 3.0 Port

The VIA EPIA-P910 is equipped with two USB 3.0 ports. Each USB 3.0 port has a maximum data transfer rate of up to 5Gb/s and is backwards compatible with the USB 2.0 specification. The USB 3.0 ports provides complete Plug and Play and hot swap capabilities for external devices. The pinouts of the USB 3.0 port are shown below.

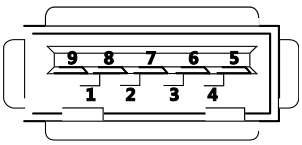

Figure 6: USB 3.0 port diagram

Pin	Signal	Pin	Signal
1	+5V	6	Rx+
2	Data-	7	GND
3	Data+	8	Tx-
4	GND	9	Tx+
5	Rx-		

Table 5: USB 3.0 port pinouts

2.1.3. Mini HDMI® Port

The integrated 19-pin mini HDMI port uses an HDMI® Type C connector as defined in the HDMI® specification. The mini HDMI port is for connecting to HDMI® displays. The pinouts of the mini HDMI port are shown below.

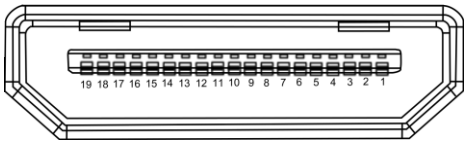

Figure 7: Mini HDMI port diagram

Pin	Signal	Pin	Signal
1	TMDS Data2 Shield	2	TMDS Data2+
3	TMDS Data2–	4	TMDS Data1 Shield
5	TMDS Data1+	6	TMDS Data1–
7	TMDS Data0 Shield	8	TMDS Data0+
9	TMDS Data0–	10	TMDS Clock Shield
11	TMDS Clock+	12	TMDS Clock–
13	DDC/CEC Ground	14	CEC
15	SCL	16	SDA
17	Reserved (N.C. on device)	18	+5V Power
19	Hot Plug Detect		

Table 6: Mini HDMI port pinouts

2.1.4. VGA Port

The 15-pin VGA port uses a female DE-15 connector. The VGA port is for connecting to analog displays. The pinouts of the VGA port are shown below.

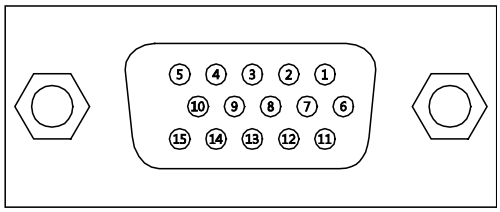

Figure 8: VGA port diagram

Pin	Signal	Pin	Signal
1	VGA-R	9	+5VCRT
2	VGA-G	10	GND
3	VGA-B	11	NC
4	NC	12	VGA-SPD
5	GND	13	VGA_HS
6	GND	14	VGA_VS
7	GND	15	VGA-SPCLK
8	GND		

Table 7: VGA port pinouts

2.2. Onboard I/O

2.2.1. LVDS Panel Connector

The VIA EPIA-P910 has one 24-pin LVDS panel connector. The LVDS panel connector connects the panel's LVDS cable to support the single-channel 18-bit/24-bit display. Backlight controls are integrated into the LVDS panel connector pinout. The LVDS panel connector is labeled as "LVDS1". The pinouts of the connector are shown below.

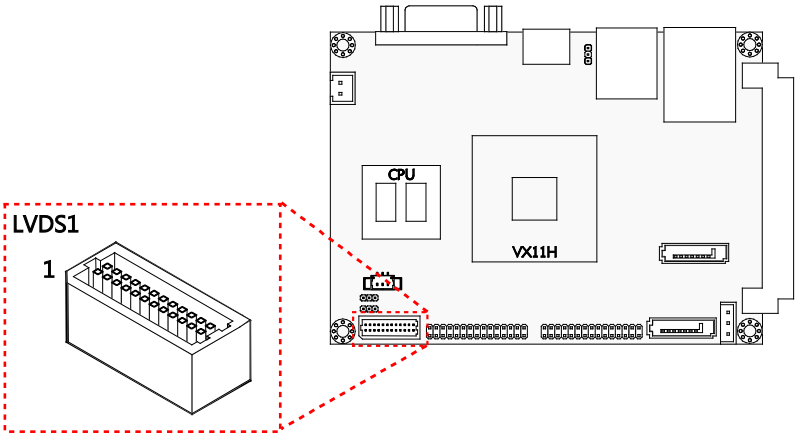

Figure 9: LVDS panel connector diagram

Pin	Signal	Pin	Signal
1	LVDSD0-	2	LVDSD1-
3	LVDSD0+	4	LVDSD1+
5	GND	6	GND
7	PVDD2	8	LVDSD2-
9	PVDD2	10	LVDSD2+
11	LCD1_DATA	12	GND
13	LCD1_CLK	14	LVDSCLK+
15	GND	16	LVDSCLK-
17	VDD_BL	18	GND
19	VDD_BL	20	LVDSD3-
21	BLEN_1	22	LVDSD3+
23	BAK_ADJ	24	GND

Table 8: LVDS panel connector pinouts

Note:

LVDS1 supports 18/24 bits EDID LCD; please ensure your LCD does support EDID. For any request of None-EDID LCD, please contact sales for customized BIOS support.

2.2.2. SATA Connectors

The two SATA connectors onboard can support up to 3Gbps transfer speeds. Both SATA connectors have a 7th pin that can provide +5V power to a SATA Disk-on-Module (DOM). When a regular SATA hard drive is connected, the 7th pin will be a ground pin. The SATA connectors are labeled as "SATA1" and "SATA2". The pinouts of the SATA connectors are shown below.

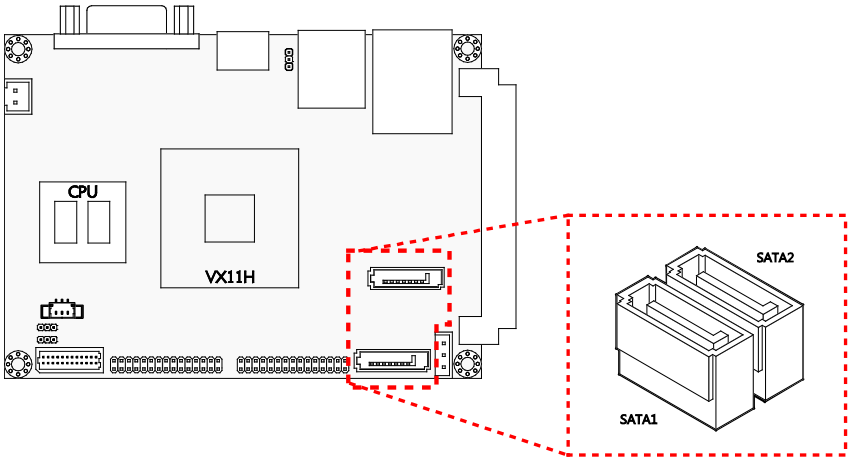

Figure 10: SATA connectors diagram

SATA1	
Pin	Signal
1	GND
2	STXP_0
3	STXN_0
4	GND
5	SRXN_0
6	SRXP_0
7	GND/+5V

SATA2	
Pin	Signal
1	GND
2	STXP_1
3	STXN_1
4	GND
5	SRXN_1
6	SRXP_1
7	GND/+5V

Table 9: SATA connectors pinouts

Note:
The SATA connector pin 7 default setting is GND. The +5V supports is a factory option.

2.2.3. SATA Power Connector

The SATA power connector provides both +5V and +12V directly through the board to the SATA drives. The SATA power connector is labeled as "PWR2". The pinouts of the SATA power connector are shown below.

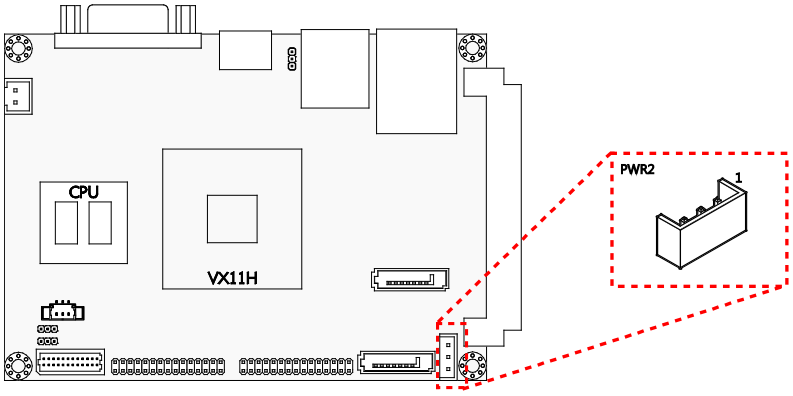

Figure 11: SATA power connector diagram

Pin	Signal
1	+5V/1A
2	+12V/1A
3	GND

Table 10: SATA power connector pinouts

2.2.4. KB/MS/LPC/GPIO/SMBus Combination Pin Header

The VIA EPIA-P910 includes one KB, MS, LPC, GPIO, and SMBus combination pin header block labeled as "CN1". The combination pin header is for connecting KB, MS, LPC, GPIO, and SMBus devices. The pinouts of the pin header are shown below.

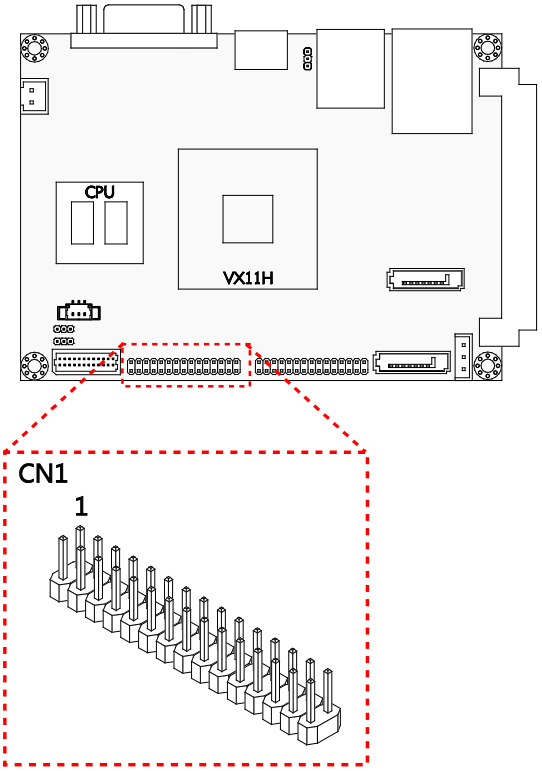

Figure 12: KB/MS/LPC/GPIO/ SMBus combination pin header diagram

Pin	Signal	Pin	Signal
1	LAD3	2	GND
3	LAD2	4	SIO_CLK1
5	LAD1	6	PCICLK3
7	-LFRAME	8	-LDRQ0
9	LAD0	10	SERIRQ
11	-PCIRST	12	GND
13	SMBDT_+3.3V	14	SMBCK_+3.3V
15	+3.3V	16	+5V
17	-LID/GPI7	18	-INTB/GPIO8
19	-THRM/GPI9	20	-INTC/GPIO9
21	-EXTSMI/GPI5	22	GPIO12/GPIO12
23	-BATLOW/GPI4	24	GPIO32/GPIO32
25	GND	26	+5VSUS
27	KBDT	28	KBCK
29	MSDT	30	MSCK

Table 11: KB/MS/LPC/GPIO/SMBus combination pin header pinouts

2.2.5. USB 2.0/Front Panel/Audio Combination Pin Header

The VIA EPIA-P910 includes one USB 2.0, Front Panel and Audio combination pin header block labeled as "CN2".The USB 2.0, front panel and audio combination pin header is used to enable up to three USB 2.0 ports and to connect the power switch, reset switch, power LED, suspend LED, HDD LED, case speaker, S/PDIF out, Line-out, Line-in and Mic-in jacks. The pinouts of the pin header are shown below.

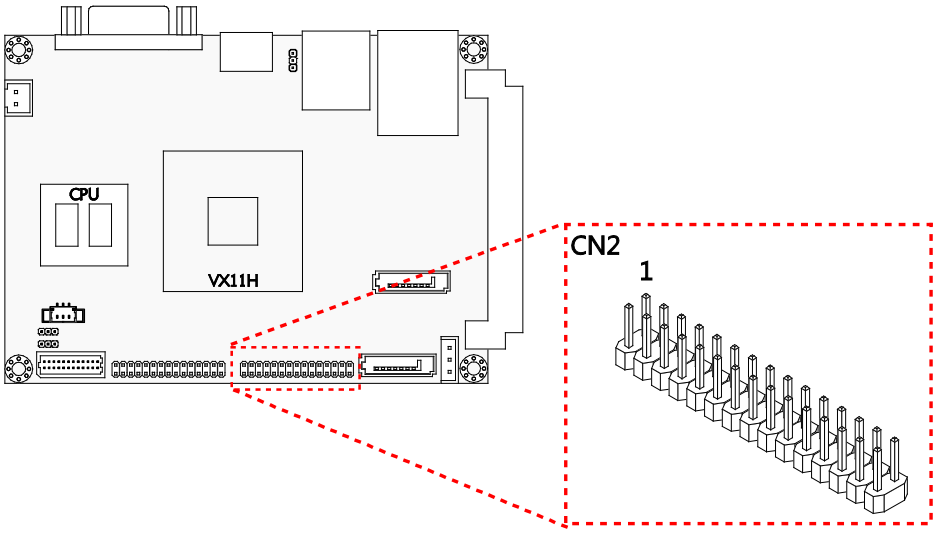

Figure 13: USB 2.0/Front panel/Audio combination pin header diagram

Pin	Signal	Pin	Signal
1	GND	2	+5VSUSH1
3	USB_VD0-	4	USB_VD0+
5	USB_VD1-	6	USB_VD1+
7	USB_VD5-	8	USB_VD5+
9	GND	10	GND
11	+5V	12	+5VSUS
13	-HD_LED	14	-PWR_LED
15	PW_BN1-	16	GND
17	GND	18	SPEAK_BZ
19	RST_SW	20	GND
21	GND_AUD	22	LINER
23	MICIN_L	24	LINEL
25	MICIN_R	26	LINEOUT_R
27	SENSE_A	28	LINEOUT_L
29	SPDIF_TX0	30	GND

Table 12: USB 2.0/Front panel/Audio combination pin header pinouts

2.2.6. System/CPU Fan Connector

The System/CPU fan connector onboard runs on +12V and maintain system/CPU cooling. The fan provides variable fan speeds controlled by the BIOS. The System/CPU fan connector is labeled as "FAN1". The pinouts of the System/CPU fan connector are shown below.

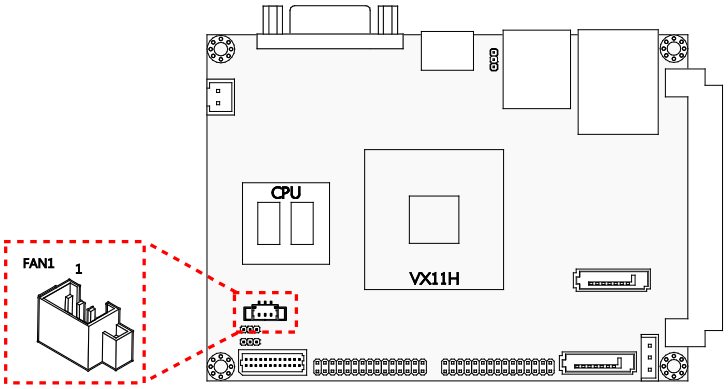

Figure 14: System/CPU fan connector diagram

Pin	Signal
1	FANIN1
2	+12V FAN
3	GND

Table 13: System/CPU fan connector pinouts

2.2.7. DC-in Power Connector

The VIA EPIA-P910 has an onboard DC-in 2-pin power connector to connect the DC-in power cable. The DC-in power connector is labeled as "PWR1". The pinouts of the DC-in power connector are shown below.

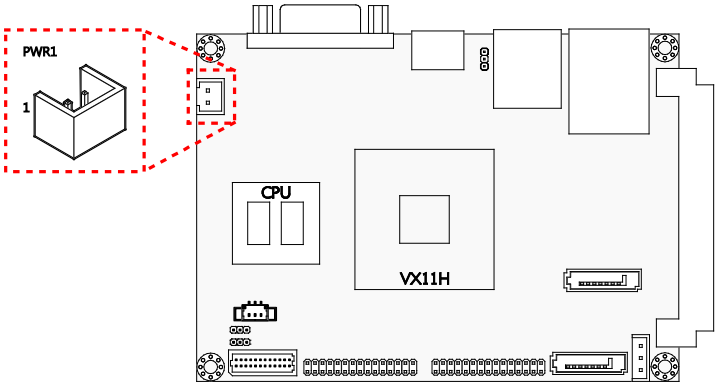

Figure 15: DC-in power connector diagram

Pin	Signal
1	+12V
2	GND

Table 14: DC-in power connector pinouts

2.2.8. CMOS Battery Connector

The VIA EPIA-P910 is equipped with CMOS battery connector used for connecting the external cable battery that provides power to the CMOS RAM. If disconnected all configurations in the CMOS RAM will be reset to factory defaults. The CMOS battery connector is labeled as "BAT1". The pinouts of the CMOS battery connector are shown below.

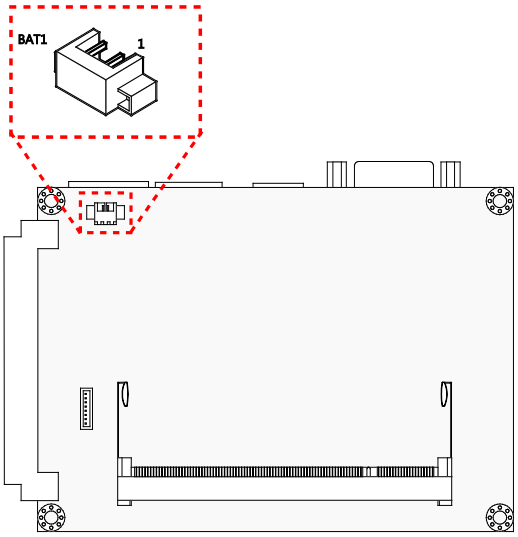

Figure 16: CMOS battery connector diagram

Pin	Signal
1	RTC_BAT
2	GND

Table 15: CMOS battery connector pinouts

2.2.9. SPI Flash Connector

The VIA EPIA-P910 has one 8-pin SPI flash connector. The SPI (Serial Peripheral Interface) flash connector is used to connect to the SPI BIOS programming fixture for updating the SPI flash ROM. The connector is labeled as "J1". The pinouts of the SPI flash connector are shown below.

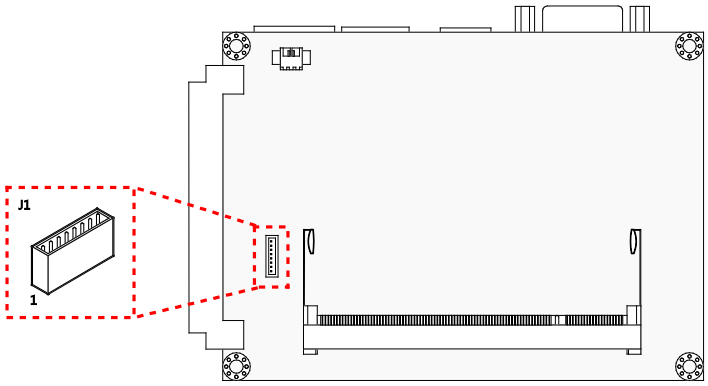

Figure 17: SPI flash connector diagram

Pin	Signal	Pin	Signal
1	NC	5	MSPICLK
2	NC	6	MSPISSO
3	MSPIDO	7	GND
4	MSPIDI	8	SPIVCC

Table 16: SPI flash connector pinouts

3. Jumpers

This section will explain how to configure the VIA EPIA-P910 to match the needs of your application by setting the jumpers.

Jumper Description

A jumper consists of a pair conductive pins used to close in or bypass an electronic circuit to set up or configure a particular feature using a jumper cap. The jumper cap is a small metal clip covered by plastic. It performs like a connecting bridge to short (connect) the pair of pins. The usual colors of the jumper cap are black/red/blue/white/yellow.

Jumper Setting

There are two settings of the jumper pin: **"Short** and **Open"**. The pins are **"Short"** when a jumper cap is placed on the pair of pins. The pins are **"Open"** if the jumper cap is removed.

In addition, there are jumpers that have three or more pins, and some pins are arranged in series. In case of a jumper with three pins, place the jumper cap on pin 1 and pin 2 or pin 2 and 3 to Short it.

Some jumpers size are small or mounted on the crowded location on the board that makes it difficult to access. Therefore, using a long-nose plier in installing and removing the jumper cap is very helpful.

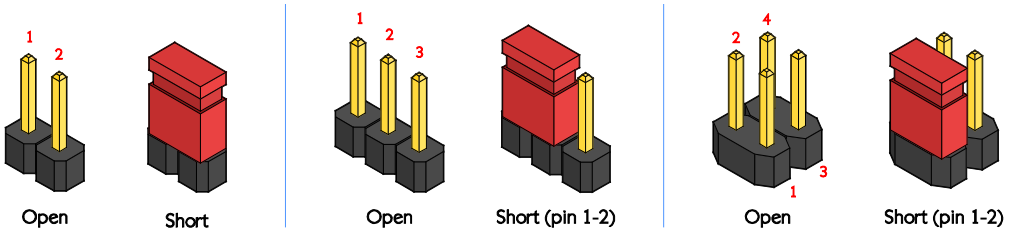

Figure 18: Jumper settings example

Caution:
Make sure to install the jumper cap on the correct pins. Installing it in the wrong pins might cause damage and malfunction.

3.1. Clear CMOS Jumper

The VIA EPIA-P910 comes with a Clear CMOS jumper The onboard CMOS RAM stores system configuration data and has an onboard battery power supply. To reset the CMOS settings, set the jumper on pins 2 and 3 while the system is off, then return the jumper to pins 1 and 2 afterwards. Setting the jumper while the system is on will damage the board. The default setting is "Short" pins 1 and 2.

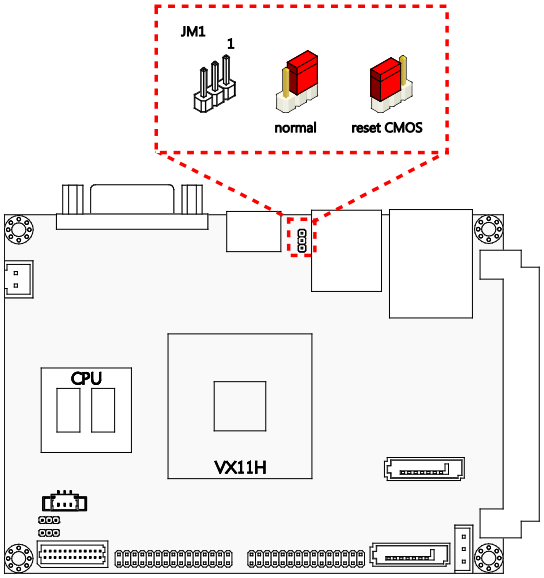

Figure 19: Clear CMOS jumper diagram

Setting	Pin 1	Pin 2	Pin 3
Normal (default)	Short	Short	Open
Clear CMOS	Open	Short	Short

Table 17: Clear CMOS jumper settings

Note:

Except when clearing the RTC RAM, never remove the cap from the Clear_CMOS jumper default position. Removing the cap will cause system boot failure. Avoid clearing the CMOS while the system is on; it will damage the board.

3.2. Backlight Power Jumper

The VIA EPIA-P910 has a jumper that controls the input voltage delivered to the LVDS inverter connector. The jumper is labeled as "JM2". The jumper settings are shown below.

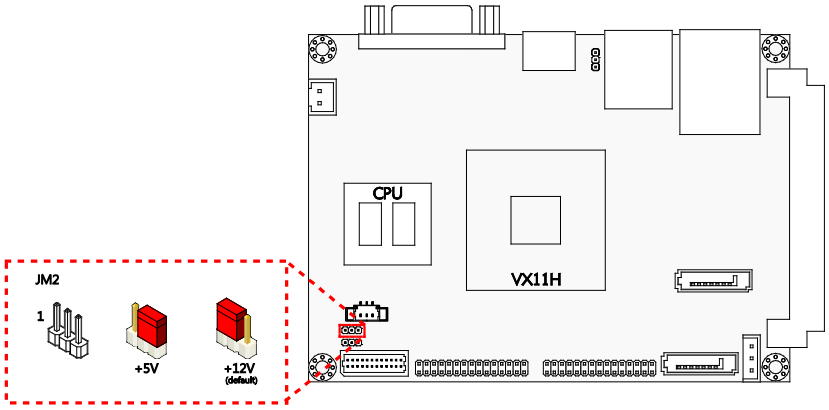

Figure 20: Backlight power jumper diagram

Setting	Pin 1	Pin 2	Pin 3
+12V (default)	Short	Short	Open
+5V	Open	Short	Short

Table 18: Backlight power jumper settings

3.3. LVDS Panel Power Jumper

The VIA EPIA-P910 has one jumper that control the voltage delivered to the LVDS panel connector. The jumper is labeled as "JM3". The jumper settings are shown below.

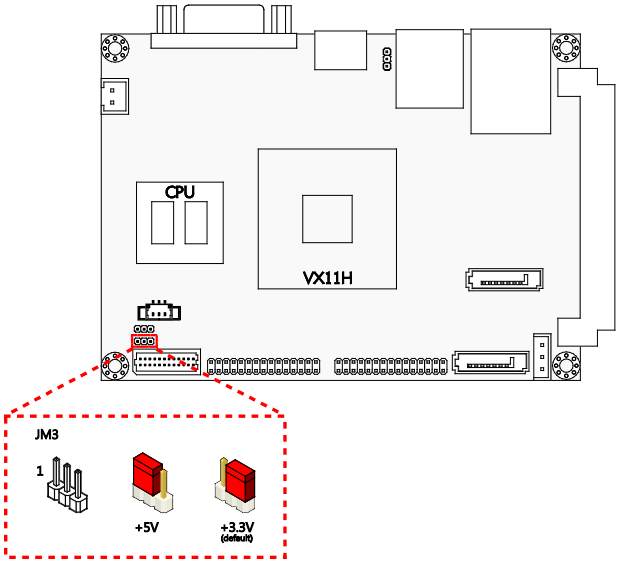

Figure 21: LVDS panel power jumper diagram

Setting	Pin 1	Pin 2	Pin 3
+3.3V (default)	Open	Short	Short
+5V	Short	Short	Open

Table 19: LVDS panel power jumper settings

4. Expansion Slots

4.1. High Speed Extension Slot

The board-to-board slot labeled as "CN3" is a combination connector reserved for connecting to a customized expansion card. The slot pinout supports PCIe, LAN, USB 2.0, Audio, SDIO and SIM.

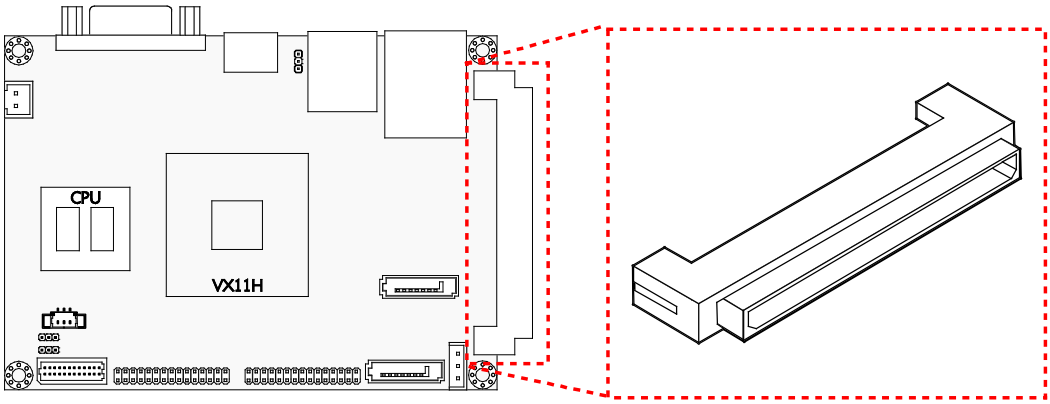

Figure 22: High Speed Extension slot diagram

Pin	Signal	Pin	Signal
1	+5VSUS	2	+5VSUS
3	+5VSUS	4	+5VSUS
5	+5VSUS	6	+5VSUS
7	+12V	8	+12V
9	GND	10	GND
11	GND	12	GND
13	GND	14	GND
15	TVCLKRIN	16	MICIN2_R
17	SPDIF_TX1	18	MICIN2_L
19	MCVREF02	20	LINE2_R
21	SENSE_B	22	LINE2_L
23	GND	24	GND
25	FANCTL2	26	SPEAK_BZ
27	FANIN2	28	GPIO37
29	-PCIRST	30	-RING
31	RST_SW	32	SD_CLK/MMC_CLK
33	PW_BN1-	34	CR_CMD
35	-SUSC	36	CR_D7
37	-SUSB	38	CR_D6
39	-CR_CD	40	CR_D5
41	-CR_WPD	42	CR_D4
43	VCCCR	44	CR_D3
45	CR_PWSELS	46	CR_D2
47	CR_PWSEL	48	CR_D1
49	CR_PWOFF	50	CR_D0
51	GND	52	GND
53	-HD_LED	54	VREFOUT_E
55	-PWR_LED	56	DVPCLKN
57	LVDSPWM1	58	DVPCLKP
59	DVPSPCLK	60	DVP1DE
61	DVPSPD	62	DVP1HS

63	SMBDT	64	DVP1VS
65	SMBCK	66	DVP1D11
67	-PEREQ1	68	DVP1D10
69	-PEXWAKE	70	DVP1D9
71	-PEX4RST	72	DVP1D8
73	-PEX2RST	74	DVP1D7
75	-PEX1RST	76	DVP1D6
77	GND	78	DVP1D5
79	USBHP3-	80	DVP1D4
81	USBHP3+	82	DVP1D3
83	GND	84	DVP1D2
85	PEXRX2+	86	DVP1D1
87	PEXRX2-	88	DVP1D0
89	GND	90	GND
91	PETN2	92	USBHP4-
93	PETP2	94	USBHP4+
95	GND	96	GND
97	PE6CLK-	98	USBHP2-
99	PE6CLK+	100	USBHP2+
101	GND	102	GND
103	PEXRX0-	104	PEXRX4-
105	PEXRX0+	106	PEXRX4+
107	GND	108	GND
109	PETN0	110	PETN4
111	PETP0	112	PETP4
113	GND	114	GND
115	PE1CLK-	116	PE3CLK-
117	PE1CLK+	118	PE3CLK+
119	GND	120	GND

Table 20: High Speed Extension slot pinouts

4.2. DDR3 SODIMM Memory Slot

The VIA EPIA-P910 provides one 204-pin DDR3 SODIMM slot that supports non-ECC DDR3 1600/1333/1066 SODIMM memory modules. The memory slot can accommodate up to 8GB of DDR3 1600/1333/1066 memory. The memory slot is labeled as "SODIMM1". The location of the DDR3 memory slot is shown below.

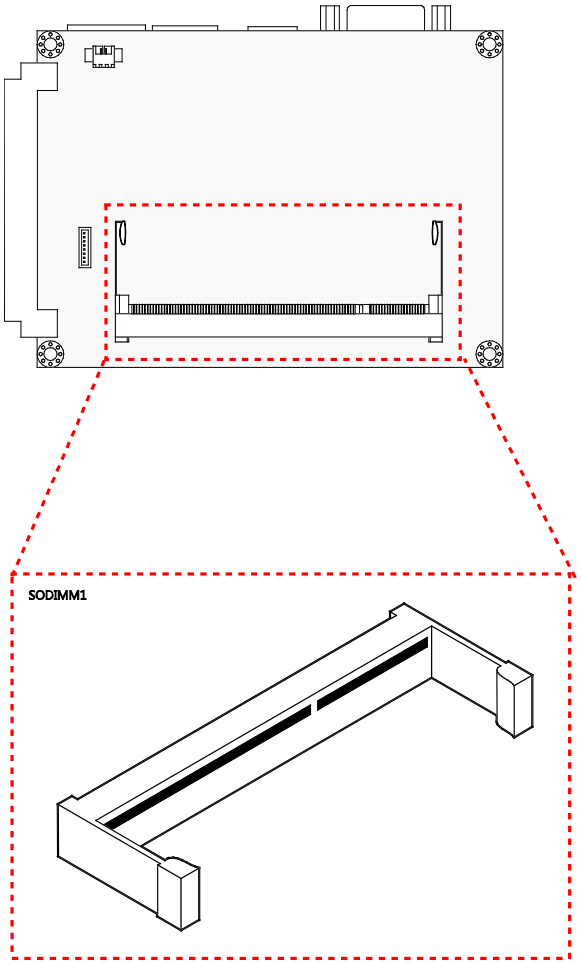

Figure 23: DDR3 SODIMM memory slot diagram

4.2.1. Installing a Memory Module

Step 1

Align the notch on the SODIMM memory module with the protruding wedge on the SODIMM memory slot. Insert the SODIMM memory module at a 30 degree angle relative to the SODIMM memory slot.

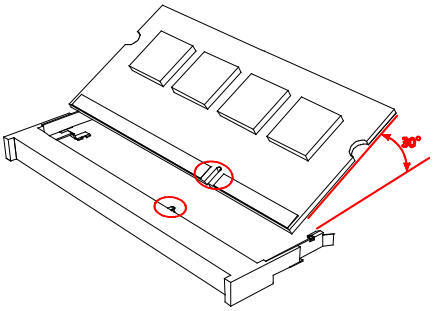

Figure 24: Inserting the memory module

Step 2

Push down the SODIMM memory module until the locking clasps lock the module into place. There will be a slight tension as the SODIMM memory module is being locked.

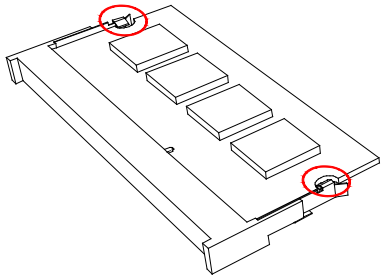

Figure 25: Locking the memory module

Step 3

Install the memory thermal pad on the top of the SODIMM memory module.

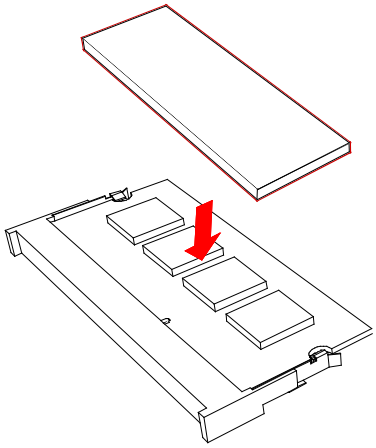

Figure 26: Installing the memory thermal pad

The memory thermal pad is used for transferring the heat dissipation of memory to the thermal plate or bottom plate to attain memory cooling, and to ensure the operating temperature of the memory module should not exceed to 85°C. This helps to prevent damage of the memory module. The memory thermal pad to be used is requires a certain thickness in order to make contact with the memory thermal plate or bottom plate to excellently disperse the heat.

Important:

1. The customer/user should consider using the memory thermal pad and adding memory thermal plate or bottom plate on their chassis design.
2. The memory thermal plate/bottom plate material to be used should have an excellent thermal conductivity. Avoid using plastic or rubber materials.
3. The thickness of memory thermal pad should be based on customer's design. However, the minimum value of thermal conductivity K (W/m.k) is 1.5 and the maximum of hardness is 5 (Shore A).

4.2.2. Removing a Memory Module

Step 1

To disengage the locking clasps, push the locking clasps horizontally outward away from the SODIMM memory module.

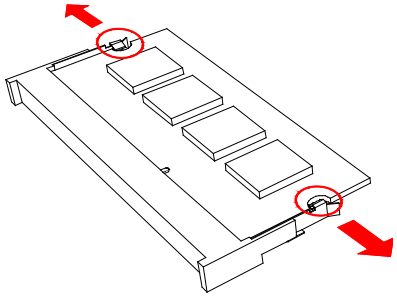

Figure 27: Disengaging the SODIMM locking clasps

Step 2

When the locking clasps have cleared, the SODIMM memory module will automatically pop up. Remove the memory module.

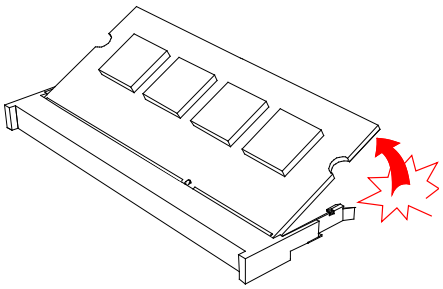

Figure 28: Removing the memory module

5. Hardware Installation

5.1. Installing the VIA EPIA-P910-A I/O Expansion Card

The optional VIA EPIA-P910-A I/O expansion card is connected through CN1 and CN2 pin headers. Align and attach the board-to-board connector on the bottom of the VIA EPIA-P910-A I/O expansion card with the CN1 and CN2 blocks on the VIA EPIA-P910.

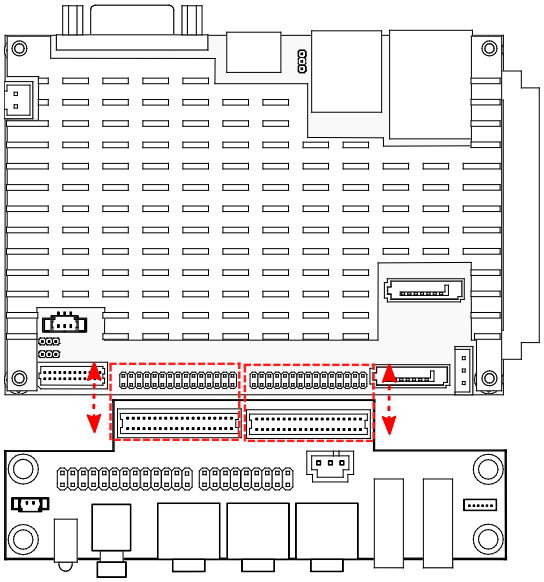

Figure 29: Connecting the VIA EPIA-P910-A I/O expansion card

Note:

The VIA EPIA-P910-A I/O expansion card is for project based enquiries only. Please contact sales for detailed information.

5.2. Installing into a Chassis

The VIA EPIA-P910 can be fitted into any chassis that has mounting holes compatible with the standard Pico-ITX mounting hole locations. Additionally, the chassis must meet the minimum height requirements for specified areas of the board.

5.2.1. Suggested minimum chassis dimensions

The figure below shows the suggested minimum space requirements that a chassis should have in order to work well with the VIA EPIA-P910.

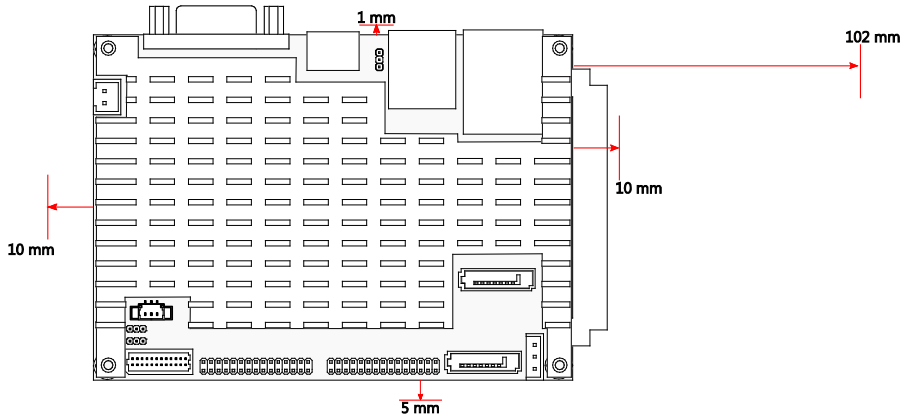

Figure 30: Suggested minimum chassis dimensions

Each side of the board should have a buffer zone from the internal wall of the chassis. The side of the board that accommodates the I/O coastline should have a buffer of 1.00mm. The side on the opposite end of the I/O coastline should have a buffer of at least 5.00mm. The two sides adjacent to the I/O coastline should have at least a 10.00mm buffer.

5.2.2. Suggested minimum chassis height

The figure below shows the suggested minimum height requirements for the internal space of the chassis. It is not necessary for the internal ceiling to be evenly flat. What is required is that the internal ceiling height must be strictly observed for each section that is highlighted.

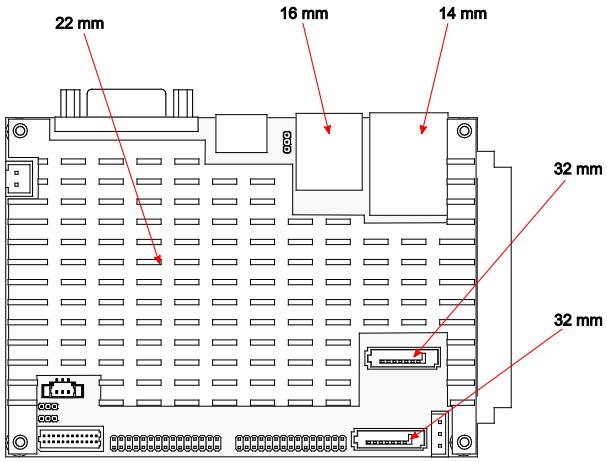

Figure 31: Suggested minimum internal chassis ceiling height

Note:

In getting the minimum height requirements for internal space of the chassis, it is required to consider the heights of the connectors (such as SPI flash connector, CMOS battery connector and DDR3 SODIMM slot) on the bottom side of the VIA EPIA-P910.

5.2.3. Suggested keepout areas

The figure below shows the areas of the board that we recommend should be left unobstructed.

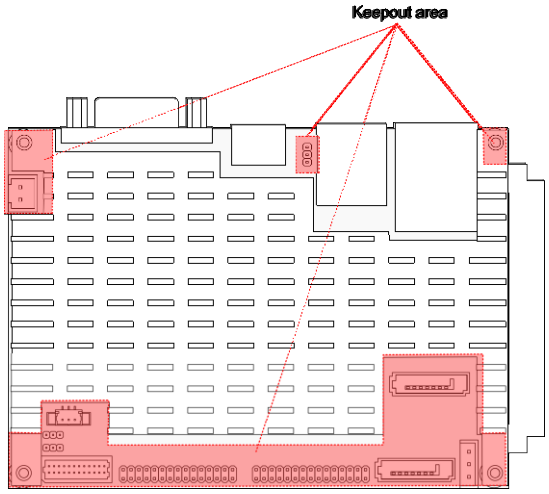

Figure 32: Suggested keepout areas

6. BIOS Setup Utility

6.1. Entering the BIOS Setup Utility

Power on the computer and press **Delete** during the beginning of the boot sequence to enter the BIOS Setup Utility. If the entry point has passed, restart the system and try again.

6.2. Control Keys

Up Move up one row

Down Move down one row

Left Move to the left in the navigation bar

Right Move to the right in the navigation bar

Enter Access the highlighted item / Select the item

Esc Jumps to the Exit screen or returns to the previous screen

+[1] Increase the numeric value

-[1] Decrease the numeric value

F1 General help[2]

F2 Previous value

F3 Load optimized defaults

F4 Save all the changes and exit

Notes:

1. Must be pressed using the 10-key pad.
2. The General help contents are only for the Status Page and Option Page setup menus.

6.3. Getting Help

The BIOS Setup Utility provides a "**General Help**" screen. This screen can be accessed at any time by pressing **F1**. The help screen displays the keys for using and navigating the BIOS Setup Utility. Press **Esc** to exit the help screen.

6.4. System Overview

The System Overview screen is the default screen that is shown when the BIOS Setup Utility is launched. This screen can be accessed by traversing the navigation bar to the "Main" label.

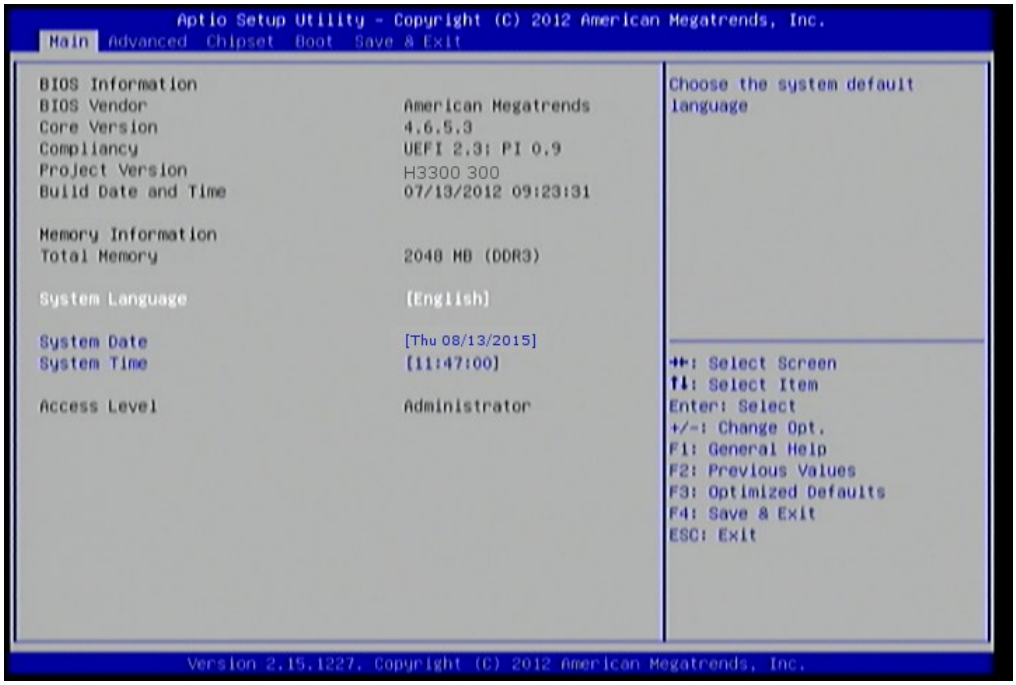

Figure 33: Illustration of the Main menu screen

6.4.1. BIOS Information

The content in this section of the screen shows the information about the vendor, the Core version, UEFI specification version, the project version and date & time of the project build.

6.4.2. Memory Information

This section shows the amount of memory that is installed on the hardware platform.

6.4.3. System Language

This option allows the user to configure the language that the user wants to use.

6.4.4. System Date

This section shows the current system date. Press **Tab** to traverse right and **Shift+Tab** to traverse left through the month, day, and year segments. The + and - keys on the number pad can be used to change the values. The weekday name is automatically updated when the date is altered. The date format is [Weekday, Month, Day, Year].

6.4.5. System Time

This section shows the current system time. Press **Tab** to traverse right and **Shift+Tab** to traverse left through the hour, minute, and second segments. The + and - keys on the number pad can be used to change the values. The time format is [Hour : Minute : Second].

6.5. Advanced Settings

The Advanced Settings screen shows a list of categories that can provide access to a sub-screen. Sub-screen links can be identified by the preceding right-facing arrowhead.

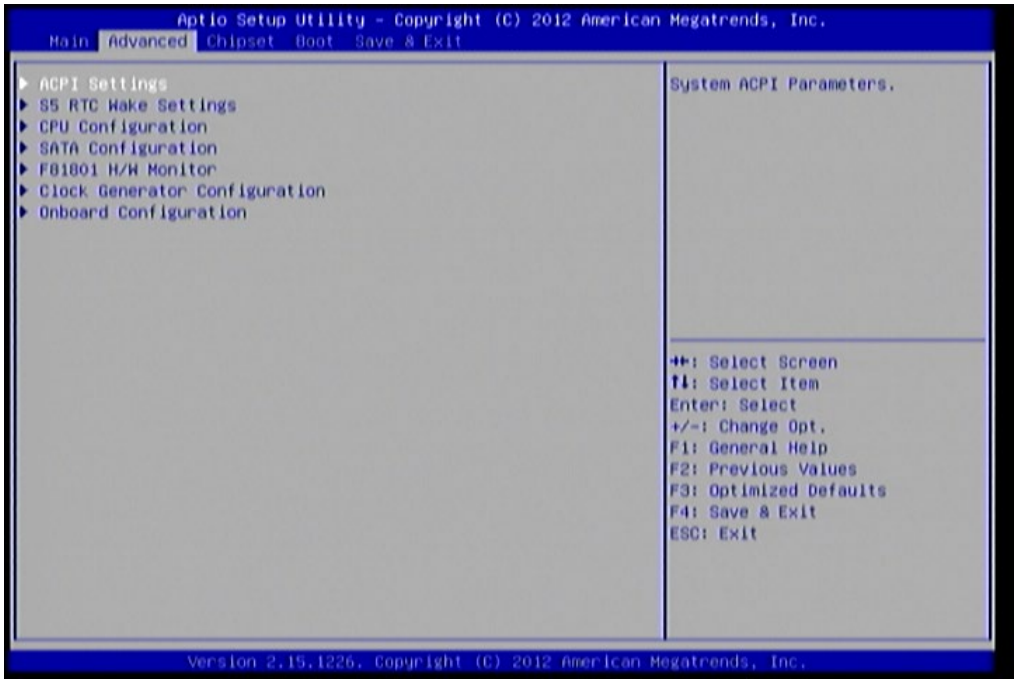

Figure 34: Illustration of the Advanced Settings screen

The Advanced Settings screen contains the following links:

- ACPI Settings
- S5 RTC Wake Settings
- CPU Configuration
- SATA Configuration
- F81801 H/W Monitor
- Clock Generator Configuration
- Onboard Configuration

6.5.1. ACPI Settings

ACPI grants the operating system direct control over system power management. The ACPI Configuration screen can be used to set a number of power management related functions.

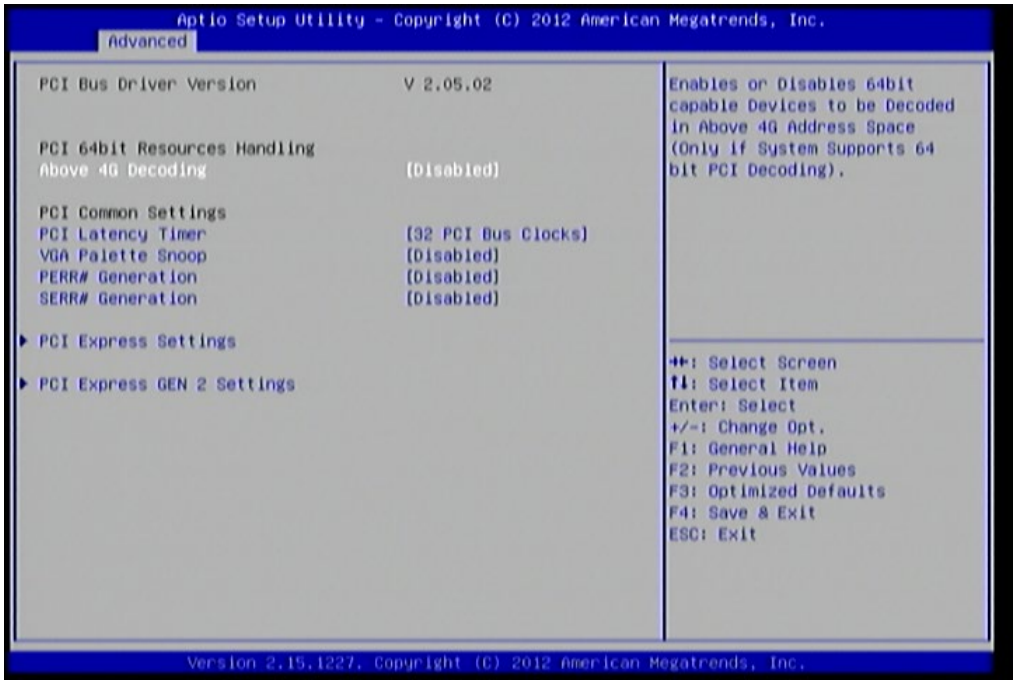

Figure 35: Illustration of the ACPI Settings screen

6.5.1.1. Enable Hibernation

Enable/disable system ability to Hibernate.

6.5.1.2. ACPI Sleep State

Select the highest ACPI sleep state the system will enter when the SUSPEND button is selected. Available options are: Suspend Disabled / S1(CPU Stop Clock) /S3 (Suspend to RAM) / Both S1 and S3 available for OS to choose.

6.5.2. S5 RTC Wake Settings

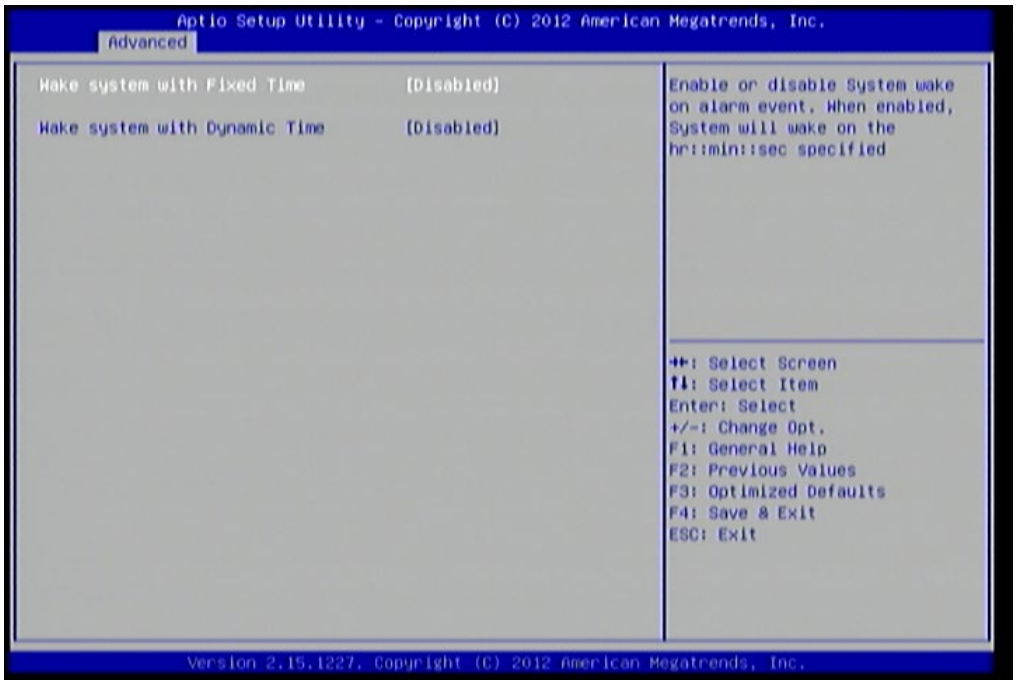

Figure 36: Illustration of the S5 RTC Wake Settings screen

6.5.2.1. Wake system with Fixed Time

Enable or disable system wake on alarm event. When enabled, system will wake on the hr:min:sec specified.

6.5.2.2. Wake system with Dynamic Time

Enable or disable Wake system with Dynamic Time.

6.5.3. CPU Configuration

The CPU Configuration screen shows detailed information about the built-in processor. In addition to the processor information, the thermal controls can be set.

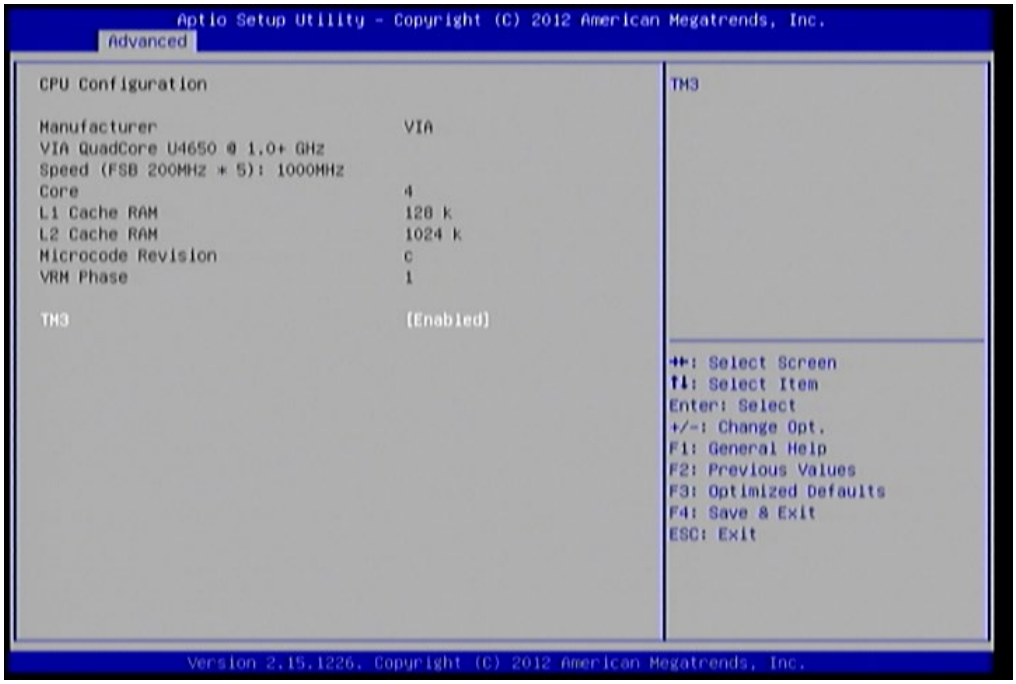

Figure 37: Illustration of CPU Configuration screen

6.5.3.1. TM3

The TM3 Function has two settings: Disabled and Enabled. When the setting is changed to "Disabled", the CPU's built-in thermal sensor will not function. When the setting is changed to "Enabled", the thermal sensor will automatically adjust the CPU ratio and V CORE to prevent the CPU from overheating.

6.5.4. SATA Configuration

The SATA Configuration screen allows the user to view and configure the settings of the SATA configuration settings.

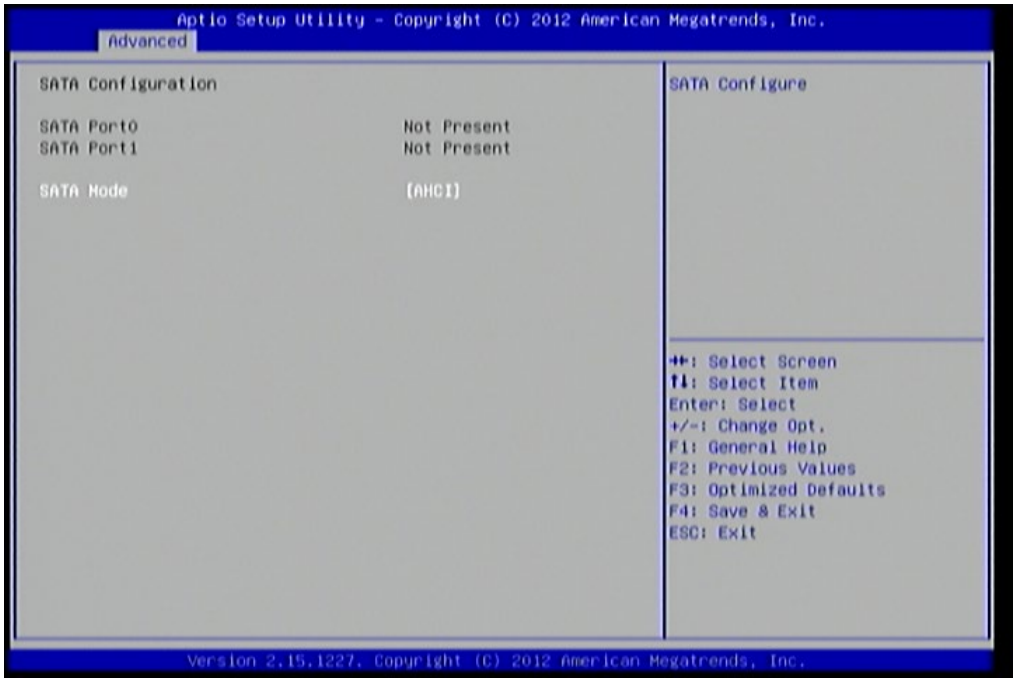

Figure 38: Illustration of SATA Configuration screen

6.5.4.1. SATA Mode

This option allows the user to manually configure SATA controller for a particular mode.

IDE Mode

Set this value to change the SATA to IDE mode.

AHCI Mode

Set this value to change the SATA to AHCI mode.

6.5.5. PC Health Status

The PC Health Status screen has no editable fields. The system temperature is taken from an optional sensor that is connected to the J5 pin header.

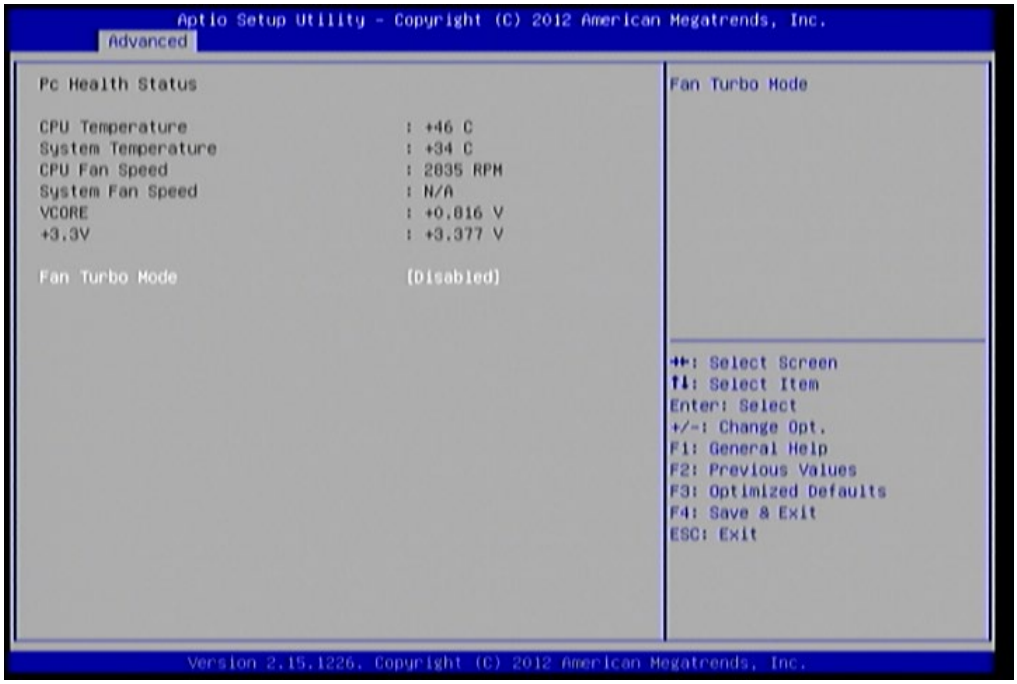

Figure 39: Illustration of PC Health Status screen

6.5.5.1. Fan Turbo Mode

This option allows the user to Enable or Disable Fan Turbo Mode.

6.5.6. Clock Generator Configuration

The Clock Generator Configuration screen enables access to the Spread Spectrum Setting feature.

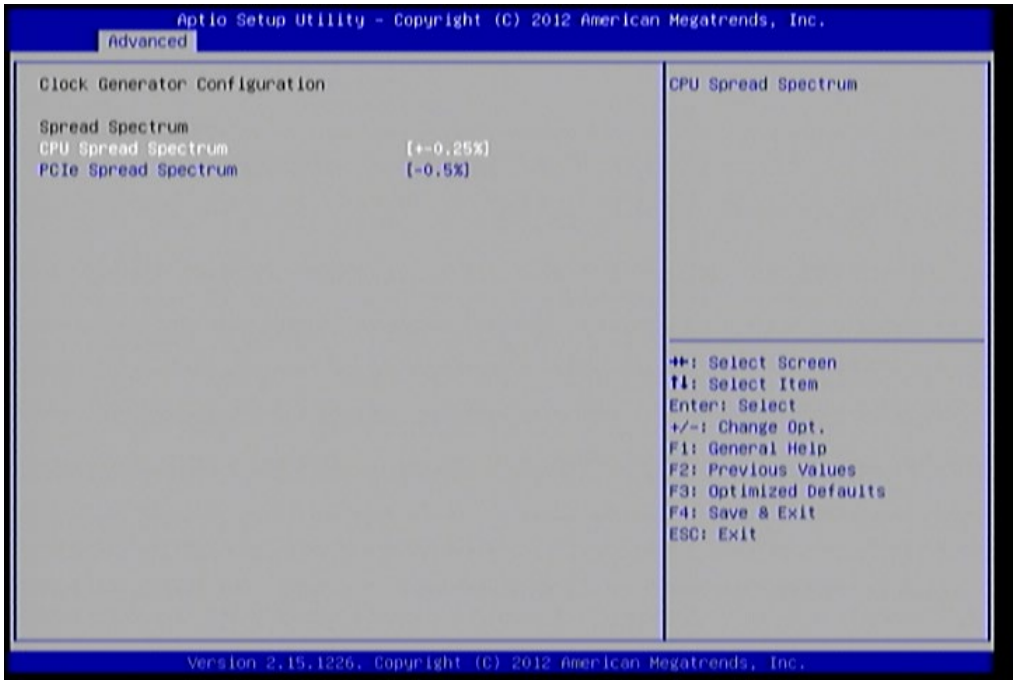

Figure 40: Illustration of Clock Generator Configuration screen

6.5.6.1. CPU Spread Spectrum

The Spread Spectrum Setting feature enables the BIOS to modulate the clock frequencies originating from the board. The settings are in percentages of modulation. Higher percentages result in greater modulation of clock frequencies. This feature has 3 options: Disable, +-0.25% and -0.5%.

6.5.6.2. PCIe Spread Spectrum

Select PCIe Spread Spectrum. This feature has 2 options: Disable and -0.5%.

6.5.7. OnBoard Device Configuration

The OnBoard Device Configuration screen has the following features.

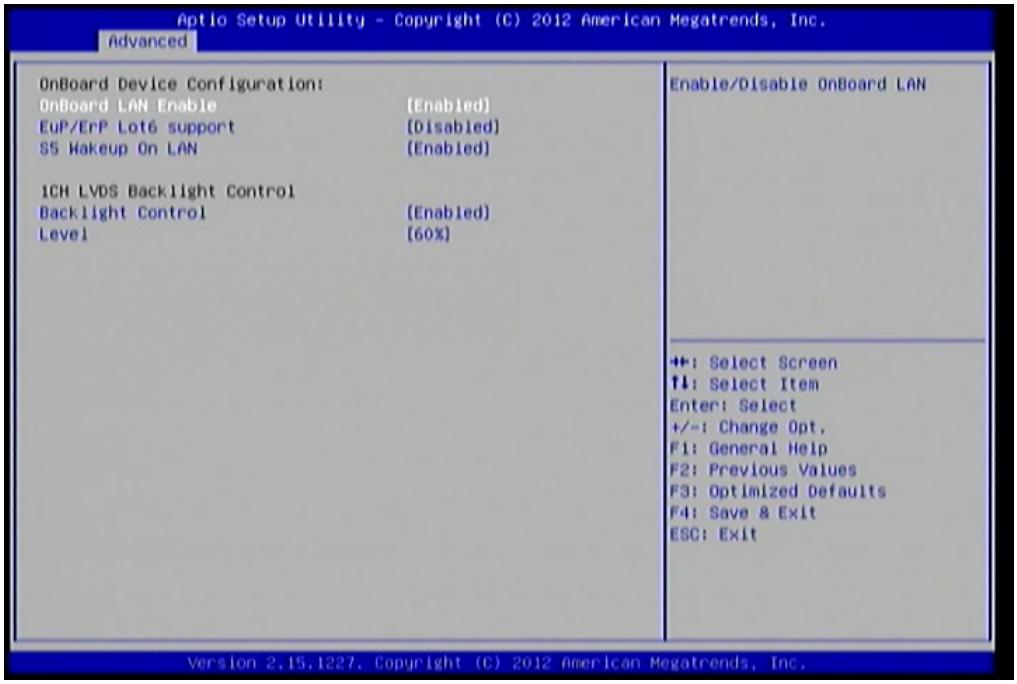

Figure 41: Illustration of OnBoard Device Configuration screen

6.5.7.1. OnBoard LAN Enable

The OnBoard LAN Enable feature determines whether the onboard LAN controller will be used or not.

6.5.7.2. EuP/ErP Lot6 support

The EuP/ErP Lot6 Support feature enables the BIOS to reduce the power draw to less than 1W when the system is in standby mode. This feature has two options: enabled and disabled.

6.5.7.3. S5 Wakeup On LAN

The S5 Wakeup On LAN feature enables the BIOS to allow remote wake-up from the S5 power off state through the PCI bus.

6.5.7.4. 1CH LVDS Backlight Control

Backlight Control

The Backlight Control feature control by VX11H enables the user to control the brightness of the 1CH LVDS backlight. This feature has six options.

Level

0%, 20%, 40%, 60%, 80% and 100%.

6.6. Chipset Settings

The Chipset Settings screen shows a list of categories that can provide access to a sub-screen. Sub-screen links can be identified by the preceding right-facing arrowhead.

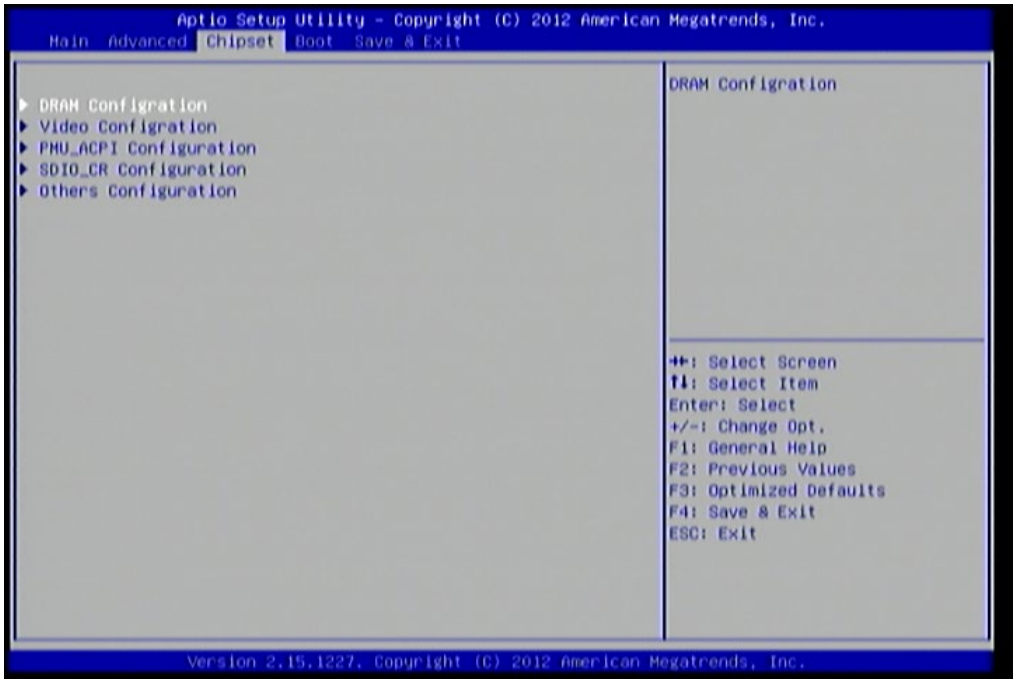

Figure 42: Illustration of Chipset Settings screen

The Chipset Settings screen contains the following links:

- DRAM Configuration
- Video Configuration
- PMU-ACPI Configuration
- SDIO_CR Configuration
- Others Configuration

6.6.1. DRAM Configuration

The DRAM Configuration screen has two features for controlling the system DRAM. All other DRAM features are automated and cannot be accessed.

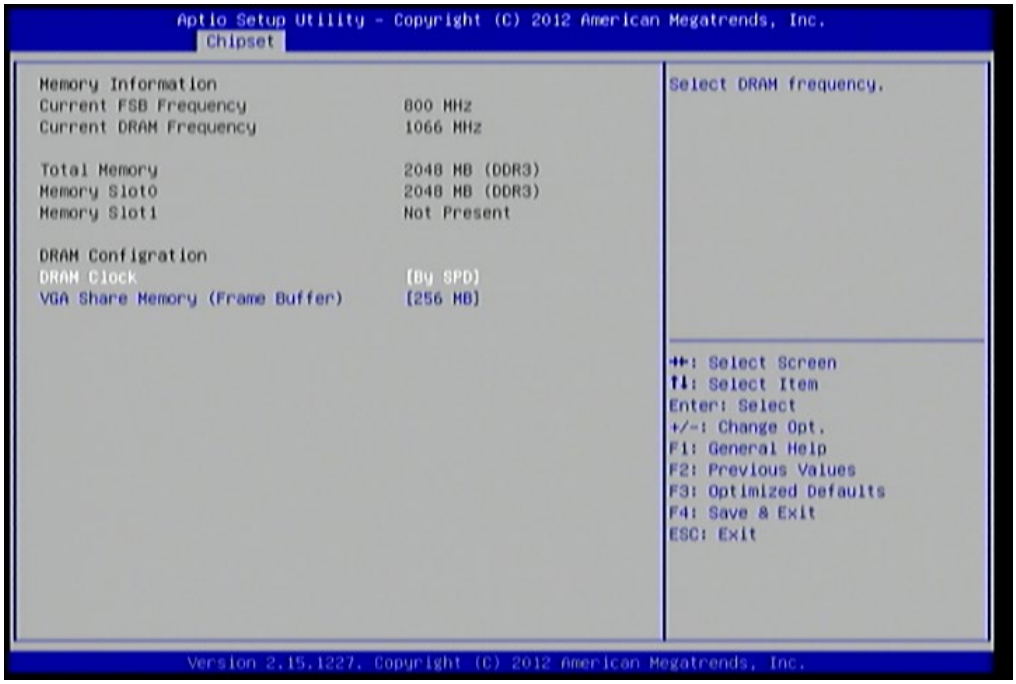

Figure 43: Illustration of DRAM Configuration screen

6.6.1.1. DRAM Clock

The DRAM Clock option enables the user to determine how the BIOS handles the memory clock frequency. The memory clock can either be dynamic or static. This feature has eleven options.

By SPD
By SPD option enables the BIOS to select a compatible clock frequency for the installed memory.

400 MHz
The 400 MHz option forces the BIOS to be fixed at 800 MHz for DDR3 memory modules.

533 MHz
The 533 MHz option forces the BIOS to be fixed at 1066 MHz for DDR3 memory modules.

566 MHz
The 566 MHz option forces the BIOS to be fixed at 1132 MHz for DDR3 memory modules.

600 MHz
The 600 MHz option forces the BIOS to be fixed at 1200 MHz for DDR3 memory modules.

633 MHz
The 633 MHz option forces the BIOS to be fixed at 1266 MHz for DDR3 memory modules.

667 MHz
The 667 MHz option forces the BIOS to be fixed at 1334 MHz for DDR3 memory modules.

6.6.1.2. VGA Share Memory (Frame Buffer)

The VGA Share Memory feature enables the user to choose the amount of the system memory to reserve for use by the integrated graphics controller. The selections of memory amount that can be reserved are 256MB and 512MB.

6.6.2. Video Configuration

The Video Configuration screen has features for controlling the integrated graphics controller in the VX11H chipset.

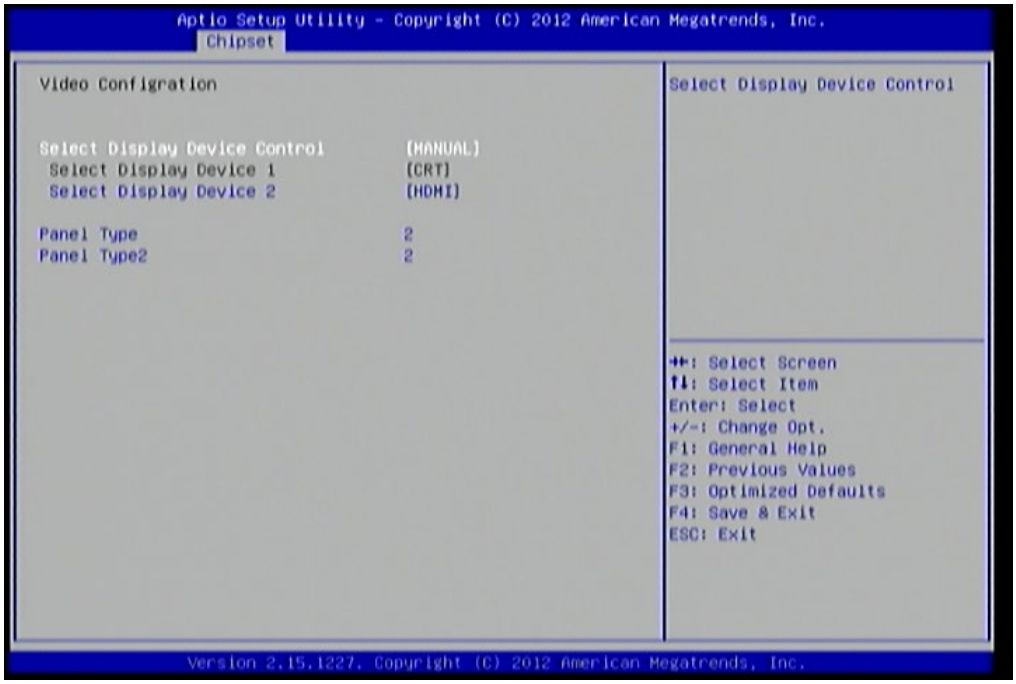

Figure 44: Illustration of Video Configuration screen

6.6.2.1. Select Display Device Control

Available selections are: Auto and Manual.

6.6.2.2. Select Display Device 1 and 2

The Select Display Device feature enables the user to choose a specific display interface. This feature has four options: CRT, LCD, LCD2 and HDMI. If both Select Display Device 1 and Select Display Device 2 are set to the same interface, then any display device connected to the other interface will not function. For example, if both Select Display 1 and 2 are set to CRT, then no data will be sent to the HDMI, LCD and LCD2 port.

6.6.2.3. Panel Type

The Panel Type feature enables the user to specify the resolution of the display being used with the system. The panel types are predefined in the VGA VBIOS.

Panel Type	Resolution	Panel Type	Resolution
00	640 x 480	08	800 x 480
01	800 x 600	09	1024 x 600
02	1024 x 768	10	1366 x 768
03	1280 x 768	11	1600 x 1200
04	1280 x 1024	12	1680 x 1050
05	1400 x 1050	13	1920 x 1200
06	1440 x 900	14	1920 x 1080
07	1280 x 800	15	1024 x 576

6.6.2.4. Panel Type2

The Panel Type feature enables the user to specify the resolution of display 2 being used with the system. The panel types are predefined in the VGA VBIOS.

Panel Type	Resolution	Panel Type	Resolution
00	640 x 480	08	800 x 480
01	800 x 600	09	1024 x 600
02	1024 x 768	10	1366 x 768
03	1280 x 768	11	1600 x 1200
04	1280 x 1024	12	1680 x 1050
05	1400 x 1050	13	1920 x 1200
06	1440 x 900	14	1920 x 1080
07	1280 x 800	15	1024 x 576

6.6.3. PMU_ACPI Configuration

The PMU_ACPI Configuration screen can be used to set a number of power management related functions.

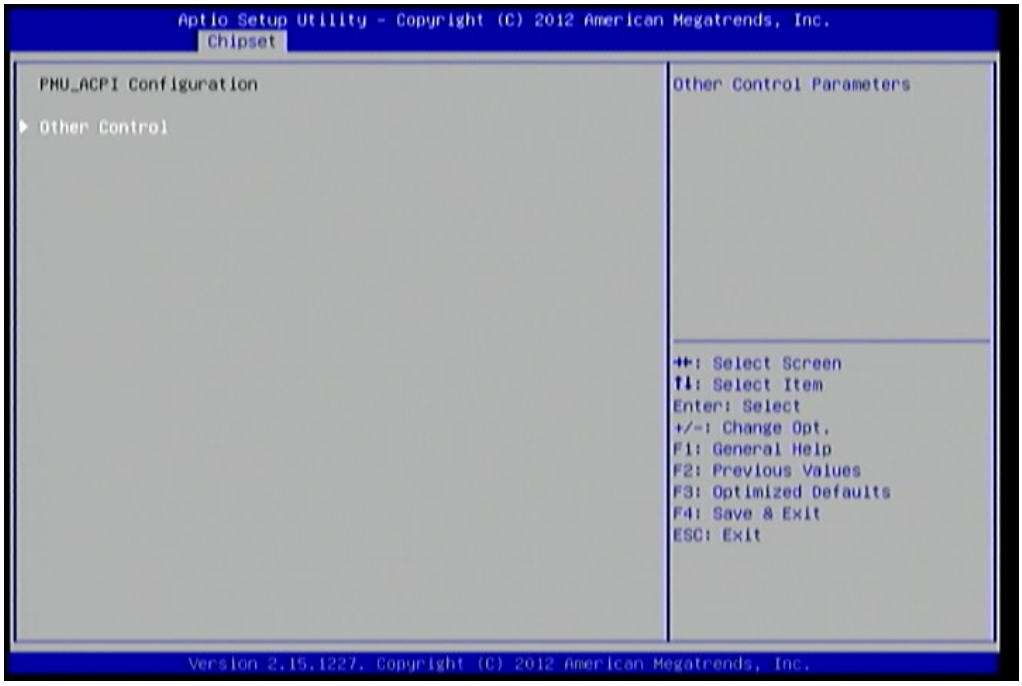

Figure 45: Illustration of PMU_ACPI Configuration screen

6.6.3.1. Other Control

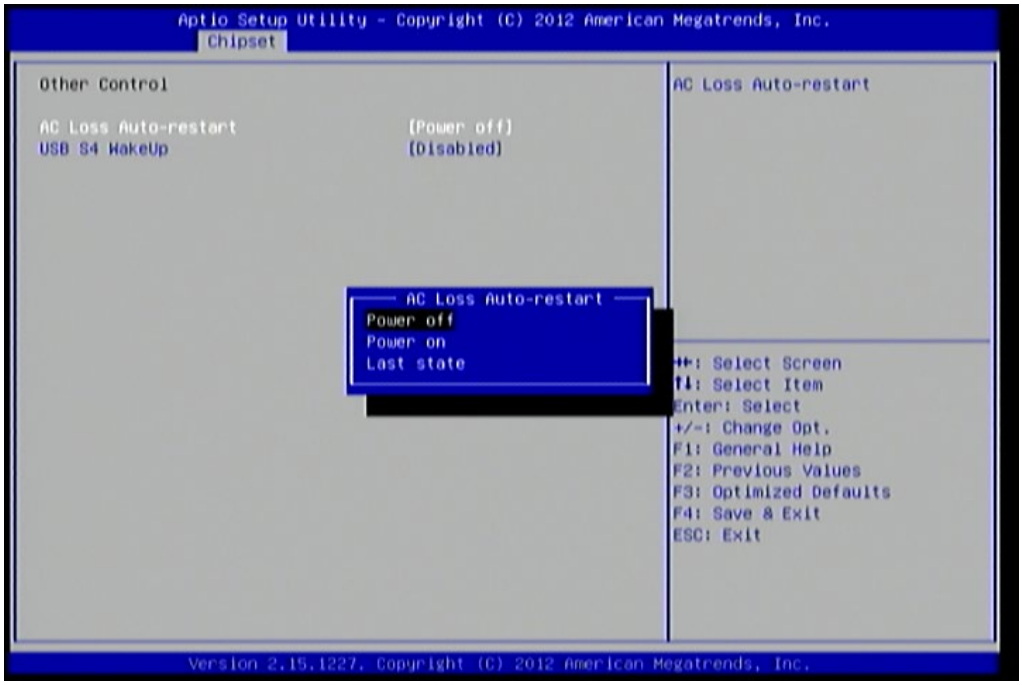

Figure 46: Illustration of Other Control screen

6.6.3.2. AC Loss Auto-restart

AC Loss Auto-restart defines how the system will respond after AC power has been interrupted while the system is on. There are three options.

Power Off
The Power Off option keeps the system in an off state until the power button is pressed again.

Power On
The Power On option restarts the system when the power has returned.

Last State
The Last State option restores the system to its previous state when the power was interrupted.

6.6.3.3. USB S4 WakeUp

The USB S4 WakeUp enables the system to resume through the USB device port from S4 state. There are two options: "Enabled" or "Disabled".

6.6.4. SDIO_CR Configuration

The SDIO_CR Configuration screen can be used to set SDIO_CR configuration parameters.

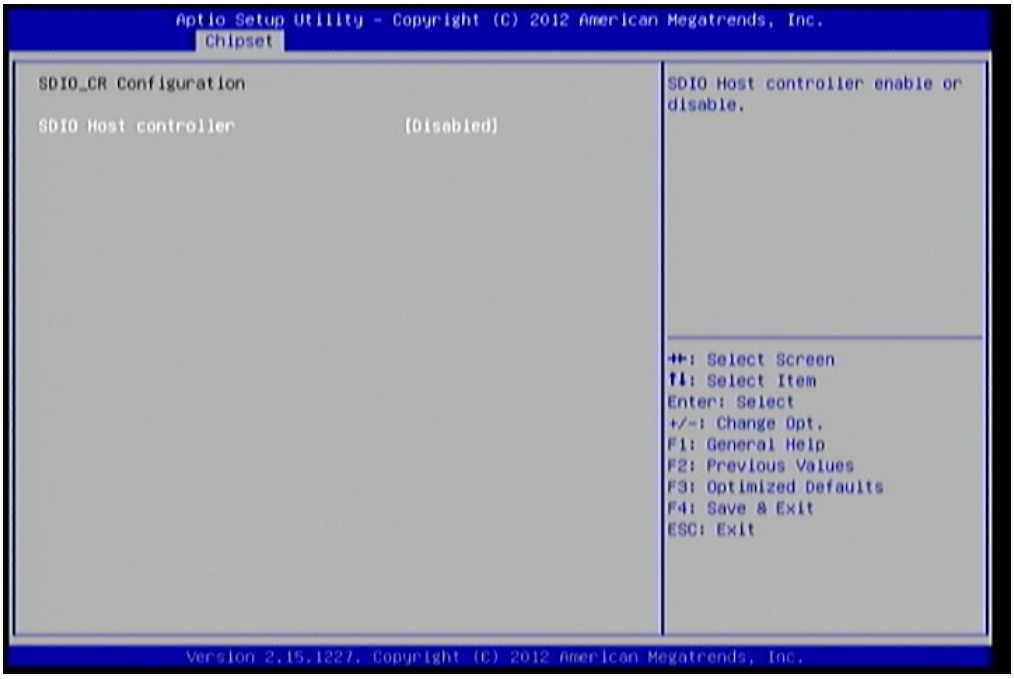

Figure 47: Illustration of SDIO_CR Configuration screen

6.6.4.1. SDIO Host Controller

Available selections are: Enabled and Disabled.

6.6.4.2. SDIO Specification Ver3.0 Support

Available selections are: Enabled and Disabled.

6.6.4.3. Voltage Support 1.8v

Available selections are: Enabled and Disabled.

6.6.4.4. High Speed Support

Available selections are: Enabled and Disabled.

6.6.4.5. Driver Type Select

Available selections are: Type A, Type B, Type C and Type D.

6.6.4.6. SDR50 Support

Available selections are: Enabled and Disabled.

6.6.4.7. SDR104 Support

Available selections are: Enabled and Disabled.

6.6.4.8. DDR50 Support

Available selections are: Enabled and Disabled.

6.6.4.9. SDR50 Tuning Enable

Available selections are: Enabled and Disabled.

6.6.4.10. Timer Count for Re-Tuning

Available selections are: 1 seconds, 2 seconds, 4 seconds, 8 seconds, 16 seconds, 32 seconds, 64 seconds, 120 seconds, 256 seconds, 512 seconds, 1024 seconds and get information from other source.

6.6.4.11. Card Reader Host Controller 0

Available selections are: Enabled and Disabled.

6.6.5. Others Configuration

The Others Configuration screen can be used to set Watchdog Timer Configuration and Keyboard/Mouse Wakeup Configuration.

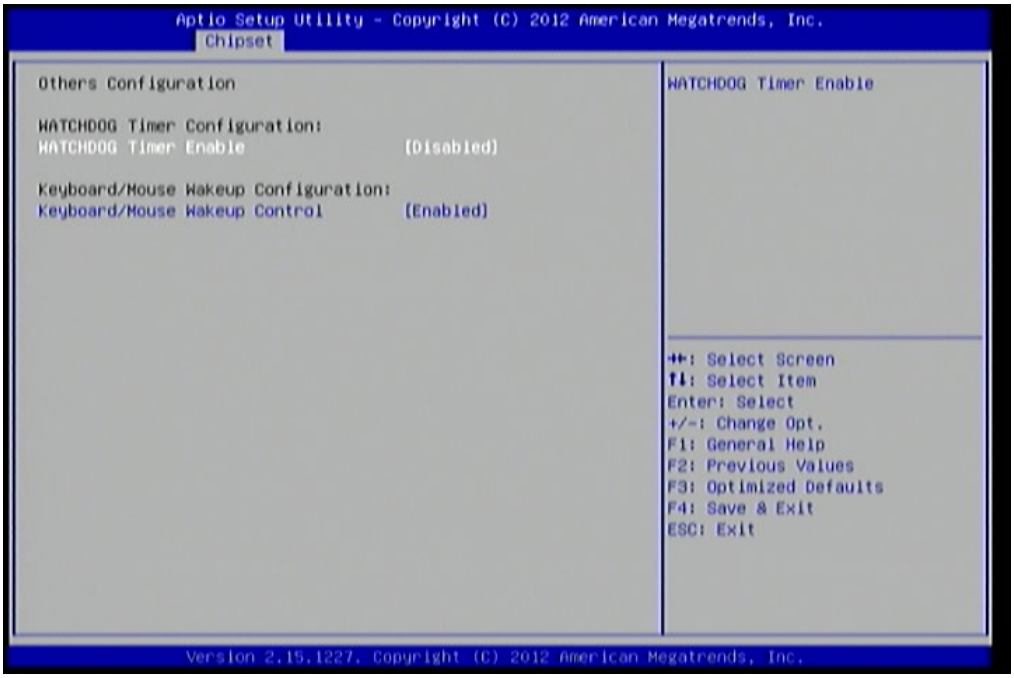

Figure 48: Illustration of Others Configuration screen

6.6.5.1. WATCHDOG Timer Enable

When this feature is enabled, an embedded timing device automatically prompts corrective action upon system malfunction detection.

6.6.5.2. Keyboard/Mouse Wakeup Control

When this feature is enabled, pressing any key of the keyboard or moving the mouse can wake up the system from suspend.

6.7. Boot Settings

The Boot Settings screen has a single link that goes to the Boot Configuration and Boot Option Priorities screens.

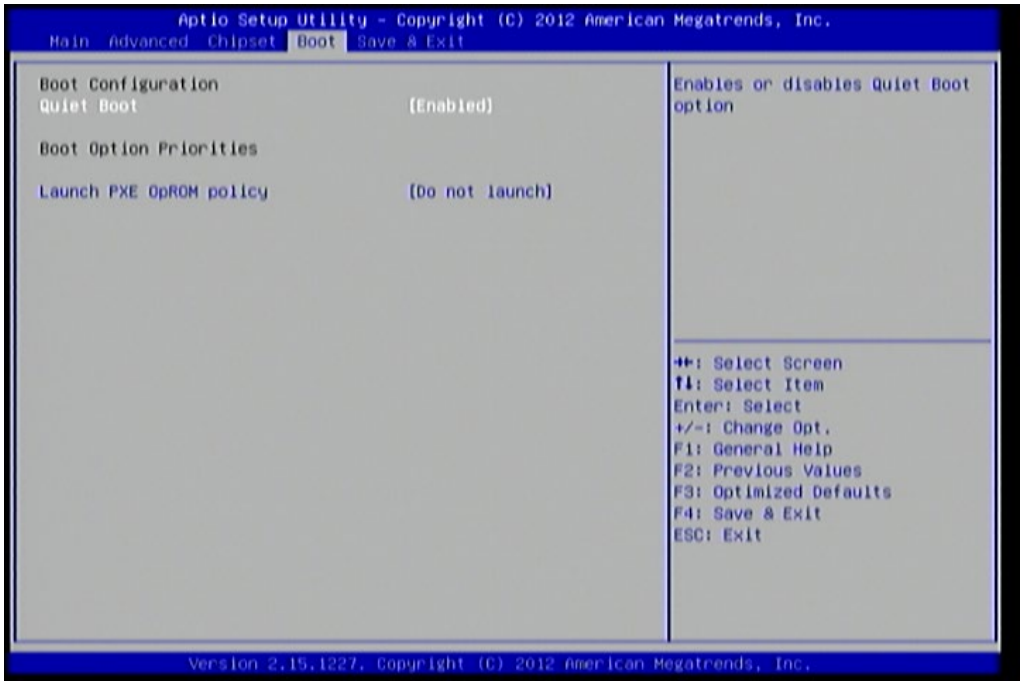

Figure 49: Illustration of Boot Settings screen

6.7.1. Boot Configuration

The Boot Settings Configuration screen has several features that can be run during the system boot sequence.

6.7.1.1. Quiet Boot

The Quiet Boot feature hides all of the Power-on Self Test (POST) messages during the boot sequence. Instead of the POST messages, the user will see an OEM logo. This feature has two options: enabled and disabled.

6.7.2. Boot Option Priorities

The Boot Option Priorities screen lists all bootable devices.

6.7.2.1. Launch PXE OpROM policy

Do not launch

Prevent the option for Legacy Network Device.

Legacy only

Allow the option for Legacy Network Device.

6.8. Save & Exit

The Save & Exit Configuration screen has the following features:

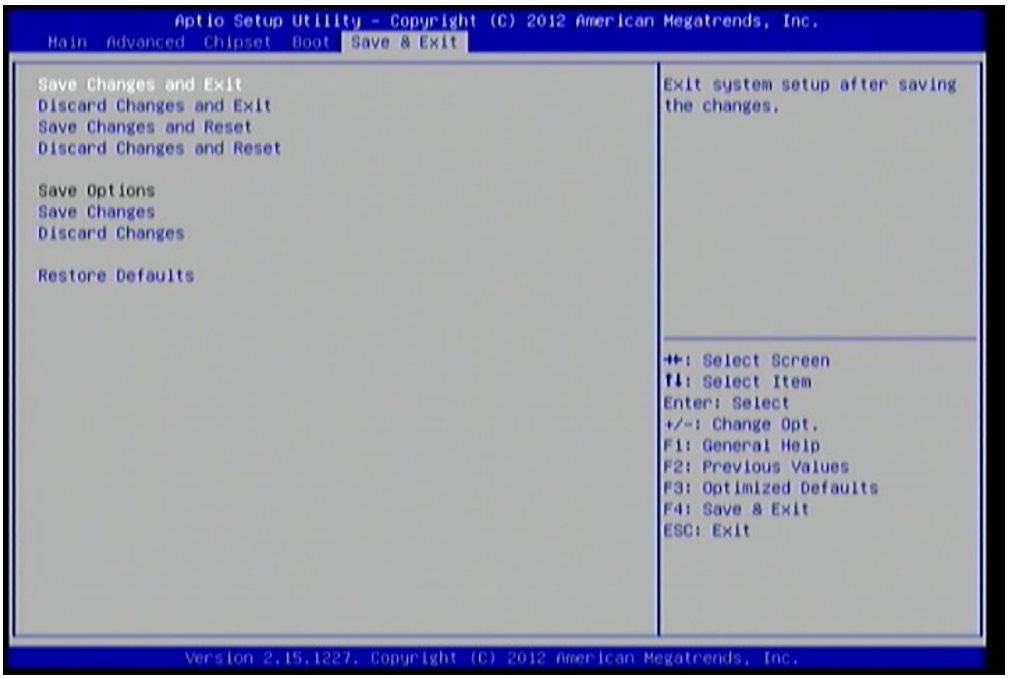

Figure 50: Illustration of Save & Exit screen

6.8.1. Save Changes and Exit

Save all changes to the BIOS and exit the BIOS Setup Utility. The "F4" hotkey can also be used to trigger this command.

6.8.2. Discard Changes and Exit

Exit the BIOS Setup Utility without saving any changes. The "Esc" hotkey can also be used to trigger this command.

6.8.3. Save Changes and Reset

Save all changes to the BIOS and reboot the system. The new system configuration parameters will take effect.

6.8.4. Discard Changes and Reset

This command reverts all changes to the settings that were in place when the BIOS Setup Utility was launched.

6.8.5. Save Options

Save Changes done so far to any of the setup options.

6.8.6. Save Changes

Save system configuration and continue. For some of the options it required to reset the system to take effect.

6.8.7. Discard Changes

Undo the previous changes.

6.8.8. Restore Defaults

Restore default values for all setup options.

7. Software and Technical Support

7.1. Microsoft and Linux Support

The VIA EPIA-P910 is compatible with Microsoft Windows and Linux operating systems.

7.1.1. Driver Installation

Microsoft Driver Support

The latest Windows drivers can be downloaded from the VIA website at www.viatech.com

Linux Driver Support

Linux drivers are provided through various methods including:

- Drivers provided by VIA (binary only). An ARCM or NDA/BSLA may be asked in order to get the drivers, please contact our sales representative to submit a request.
- Using a driver built into a distribution package
- Visiting www.viatech.com for the latest updated drivers
- Installing a third party driver (such as the ALSA driver from the Advanced Linux Sound Architecture project for integrated audio)

7.2. Technical Support and Assistance

- For utilities downloads, latest documentation and information about the VIA EPIA-P910, please visit our website at http://www.viatech.com/en/boards/pico-itx/epia-p910/
- For technical support and additional assistance, always contact your local sales representative or board distributor, or go to https://www.viatech.com/en/support/technical-support for technical support.
- For OEM clients and system integrators developing a product for long term production, other code and resources may also be made available. Please visit our website at https://www.viatech.com/en/about/contact to submit a request.

Appendix A. Installing Wireless Accessories

This chapter provides you with information on how to install the VIA EMIO wireless module into the VIA EPIA-P910. It is recommended to use a grounded wrist strap before handling computer components. Electrostatic discharge (ESD) can damage some components.

A.1. Installing the VIA EMIO-1533 USB Wi-Fi Module

Step 1

Mount the VIA EMIO-1533 module to the prepared standoff in the chassis. Align the two mounting holes on the VIA EMIO-1533 module with the mounting holes on the standoffs. And then secure the VIA EMIO-1533 module in place with two screws.

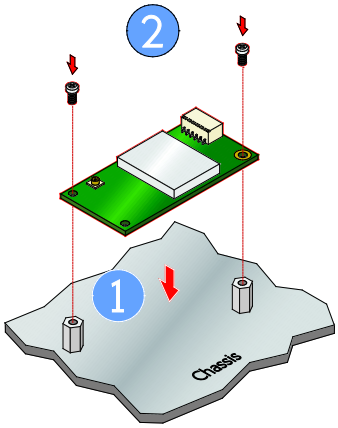

Figure 51: Installing the VIA EMIO-1533 module to the chassis

Step 2

Connect one end of USB Wi-Fi cable to the onboard USB 2.0 connector (WLAN) on VIA EPIA-P910-A I/O expansion card, and then connect the other end of the cable to the VIA EMIO-1533 module.

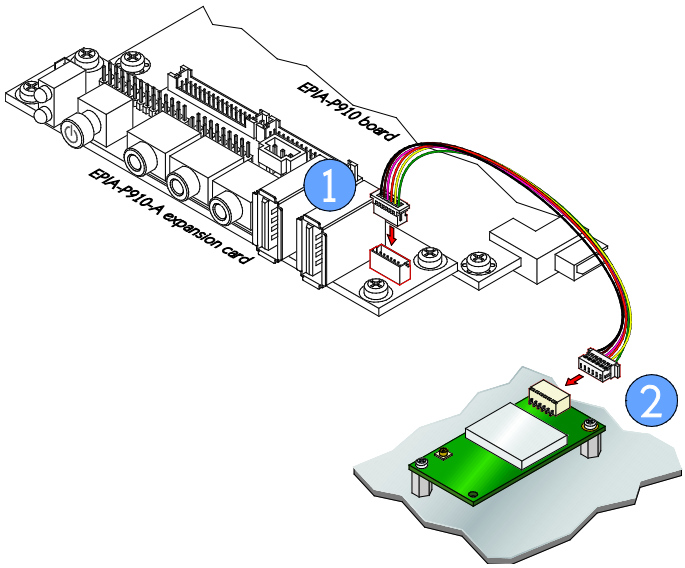

Figure 52: Connecting the USB Wi-Fi cable (VIA EMIO-1533)

Note:
Make sure the VIA EPIA-P910-A I/O expansion card is installed on the VIA EPIA-P910 before installing the VIA EMIO-1533 module.

Step 3

Insert the Wi-Fi antenna cable into the antenna hole from inside of the panel I/O plate. Insert the toothed washer, fasten it with the nut, and install the external antenna.

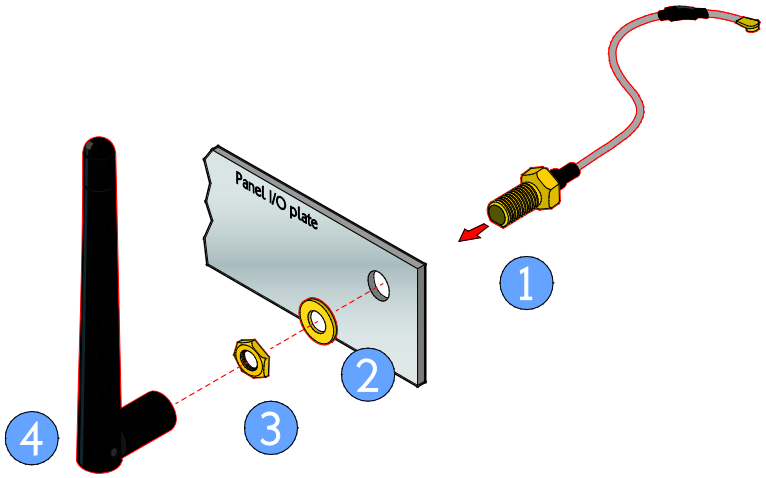

Figure 53: Installing the Wi-Fi antenna cable (VIA EMIO-1533)

Step 4

Connect the other end of the Wi-Fi antenna cable to the micro-RF connector labeled "I-PEX" on the VIA EMIO-1533 module.

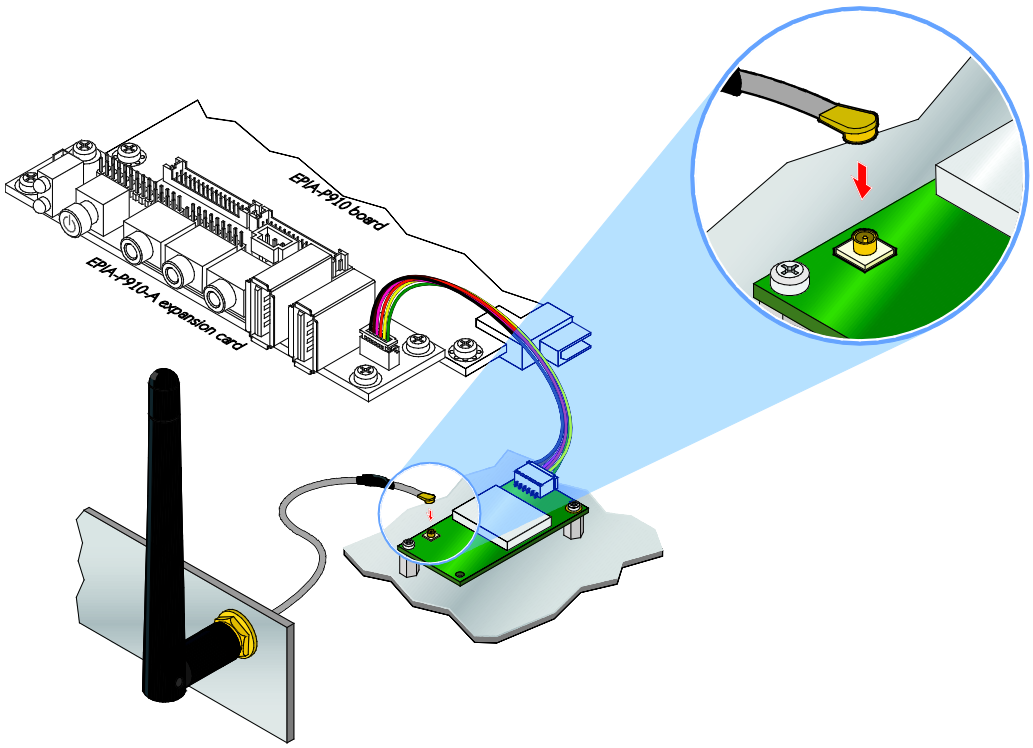

Figure 54: Connecting the Wi-Fi antenna cable to the VIA EMIO-1533 module

A.2. Installing the VIA EMIO-5531 USB Wi-Fi & Bluetooth Module

Step 1

Mount the VIA EMIO-5531 module to the prepared standoff in the chassis. Align the two mounting holes on the VIA EMIO-5531 module with the mounting holes on the standoffs, and then secure the VIA EMIO-5531 module in place with two screws.

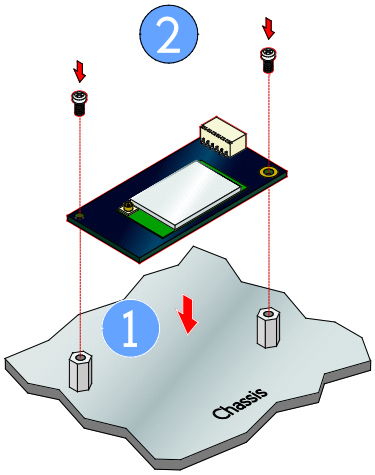

Figure 55: Installing the VIA EMIO-5531 module to the chassis

Step 2

Connect one end of USB Wi-Fi cable to the onboard USB 2.0 connector (WLAN) on VIA EPIA-P910-A I/O expansion card, and then connect the other end of the cable to the VIA EMIO-5531 module.

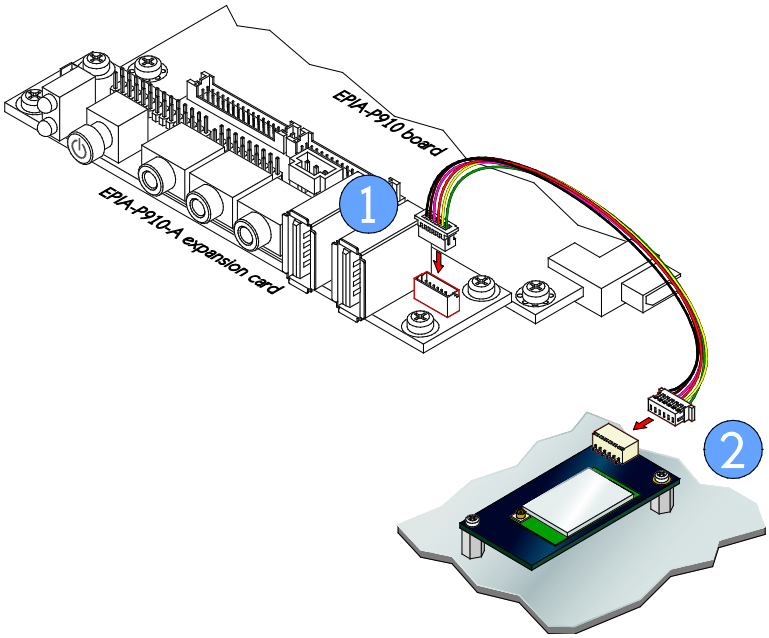

Figure 56: Connecting the USB Wi-Fi cable (VIA EMIO-5531)

Note:

Make sure the VIA EPIA-P910-A I/O expansion card is installed on the VIA EPIA-P910 before installing the VIA EMIO-5531 module.

Step 3

Insert the Wi-Fi antenna cable into the antenna hole from inside of the panel I/O plate. Insert the toothed washer, fasten it with the nut, and install the external antenna.

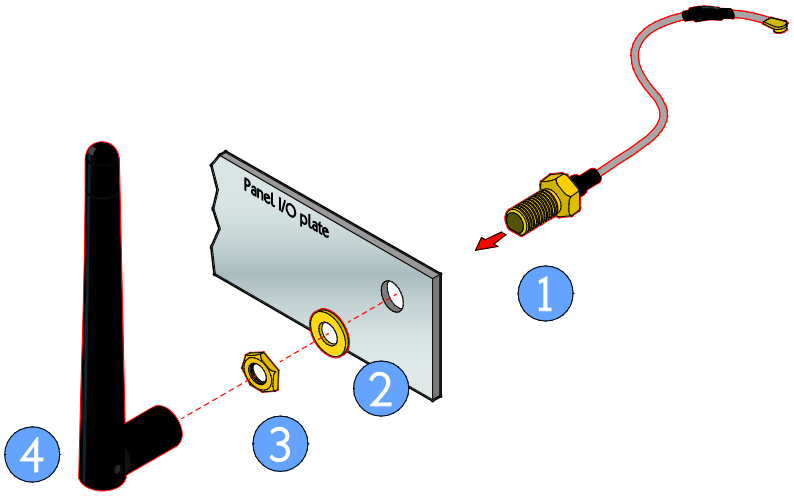

Figure 57: Installing the Wi-Fi antenna cable (VIA EMIO-5531)

Step 4

Connect the other end of the Wi-Fi antenna cable to the micro-RF connector labeled "I-PEX" on the VIA EMIO-5531 module.

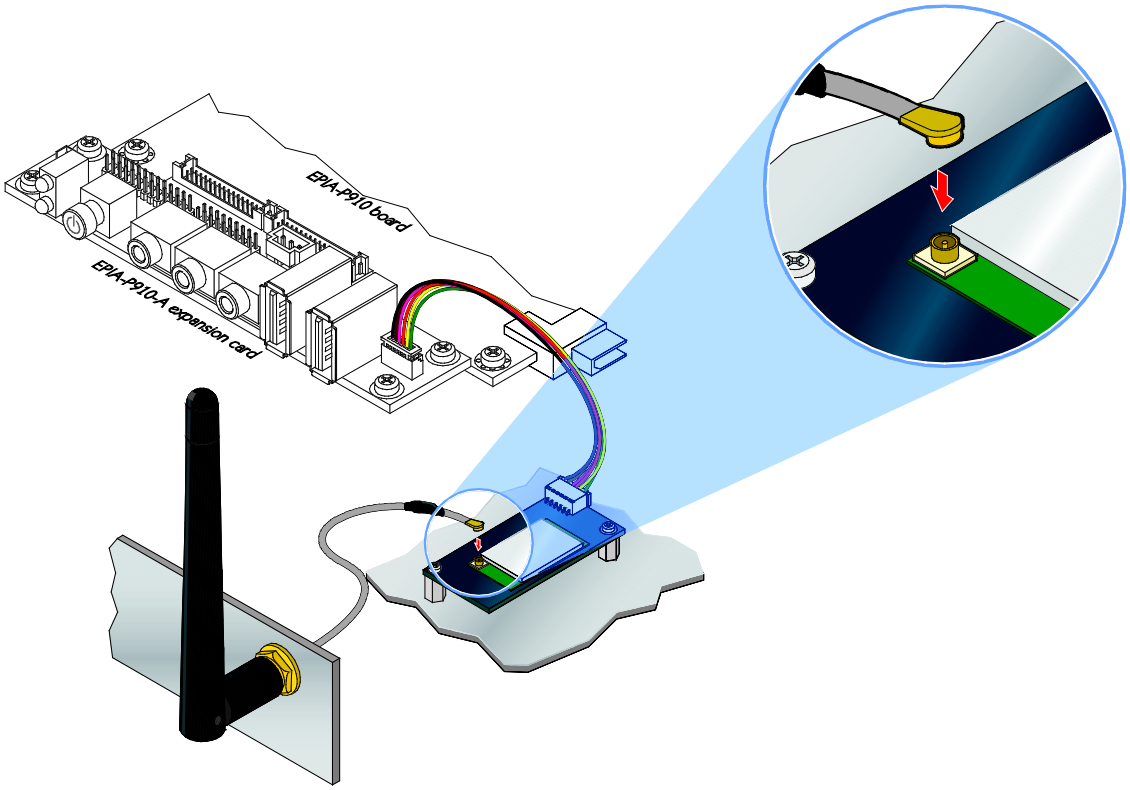

Figure 58: Connecting the Wi-Fi antenna cable to the VIA EMIO-5531 module

Appendix B. Pin Header and Connector Vendors List

The following table listed the pin header and connector vendors list of VIA EPIA-P910.

Label	Function	Pins	Vendor	Part No.
CN3	High Speed Extension slot	120	SAMTEC	ERF8-060-01-L-D-EM2-TR
CN1	KB/MS/LPC/GPIO/SMBus combination pin header	30	PINREX	232-97-15GBEB
CN2	Audio+USB 2.0+Front Panel combination pin header	30	PINREX	232-97-15GBEB
LVDS1	LVDS panel connector	24	ACES	87216-2416-06
JM2	Backlight power jumper	3	Neltron	2199SA-03G-301523
JM3	LVDS panel power jumper	3	Neltron	2199SA-03G-301523
J1	SPI flash connector	8	Neltron	1600S-08-SM-TR
JM1	Clear CMOS jumper	3	Neltron	2199SA-03G-301523
BAT1	CMOS battery connector	2	Neltron	1251R-02-SM1-TR-F5
PWR2	SATA power connector	3	Neltron	2317SEH-03
PWR1	DC-in power connector	2	Neltron	2317SJ-02-F4
FAN1	System/CPU fan connector	3	Neltron	1251S-03-SM1-TR-F5

Table 21: VIA EPIA-P910 pin header and connector vendors list

Appendix C. Power Consumption Report

Power consumption tests were performed on the VIA EPIA-P910. The following tables represent the breakdown of the voltage, ampere and wattage values while running common system applications.

C.1. EPIA-P910-12QE

The tests were performed based on the following additional components:

- **CPU:** VIA Eden X4 C4250@1.2GHz
- **Chipset:** VX11H
- **Memory:** Transcend TS512MSK64V3N-I/4GB
- **HDD SATA:** WD WD2500BEVT-00A23T0 S/NWX31A1023513
- **Power supply:** FSP GROUP INC.
  Model No. FSP060-DBAB1
  AC Input: 100~240V, 1.5A, 50~60Hz
  DC Output: 12.0V = 5.0A MAX 60W
- **Operating System:** Windows 7 + SP1 x64

C.1.1. Burn-in 3DMark06, 1920x1080 (Demo mode)

Test Condition	Volts	Amperes	Watts
Maximum	12.18	1.368	16.662
Average	12.18	1.13	13.763
Minimum	12.18	0.904	11.011

C.1.2. PassMark Burn-in (CPU usage = 100%)

Test Condition	Volts	Amperes	Watts
Maximum	12.18	1.336	16.272
Average	12.18	1.198	14.591
Minimum	12.18	1.00	12.18

C.1.3. Power DVD 10.0 to Player H.264 1080P Movie (Enable H/W Acceleration)

Test Condition	Volts	Amperes	Watts
Maximum	12.18	1.344	16.370
Average	12.18	1.13	13.763
Minimum	12.18	0.848	10.329

C.1.4. Idle at Windows 7 x64

Test Condition	Volts	Amperes	Watts
Maximum	12.18	0.864	10.524
Average	12.18	0.79	9.622
Minimum	12.18	0.768	9.354

Taiwan Headquarters

1F, 531 Zhong-zheng Road,
Xindian Dist., New Taipei City 231
Taiwan

Tel: 886-2-2218-5452
Fax: 886-2-2218-9860
Email: embedded@via.com.tw

USA

940 Mission Court
Fremont, CA 94539,
USA

Tel: 1-510-687-4688
Fax: 1-510-687-4654
Email: embedded@viatech.com

Japan

3-15-7 Ebisu MT Bldg. 6F,
Higashi, Shibuya-ku
Tokyo 150-0011
Japan

Tel: 81-3-5466-1637
Fax: 81-3-5466-1638
Email: embedded@viatech.co.jp

China

Tsinghua Science Park Bldg. 7
No. 1 Zongguancun East Road,
Haidian Dist., Beijing, 100084
China

Tel: 86-10-59852288
Fax: 86-10-59852299
Email: embedded@viatech.com.cn

Europe

Email: embedded@via-tech.eu